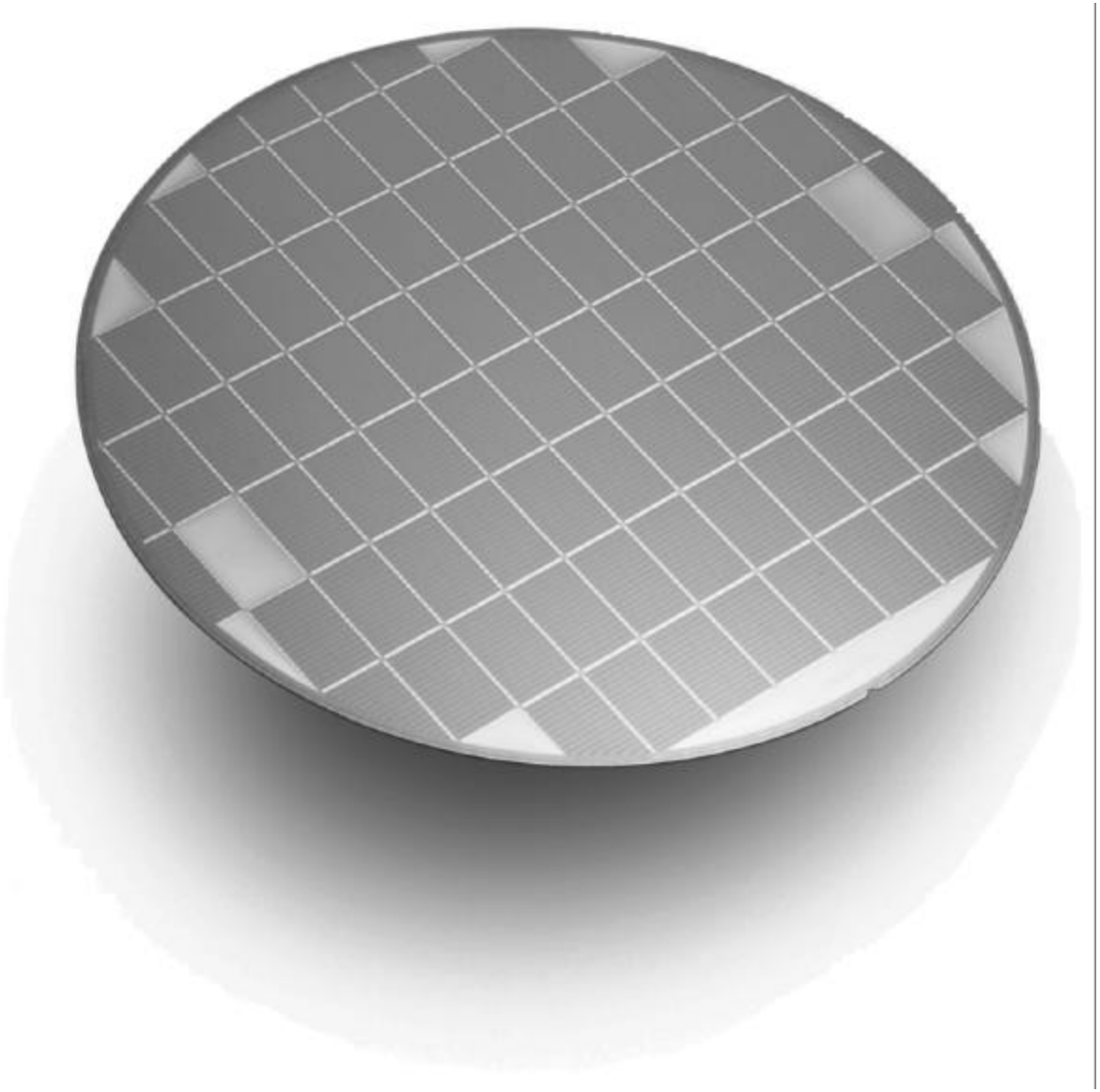

Figure 1.1 A silicon wafer

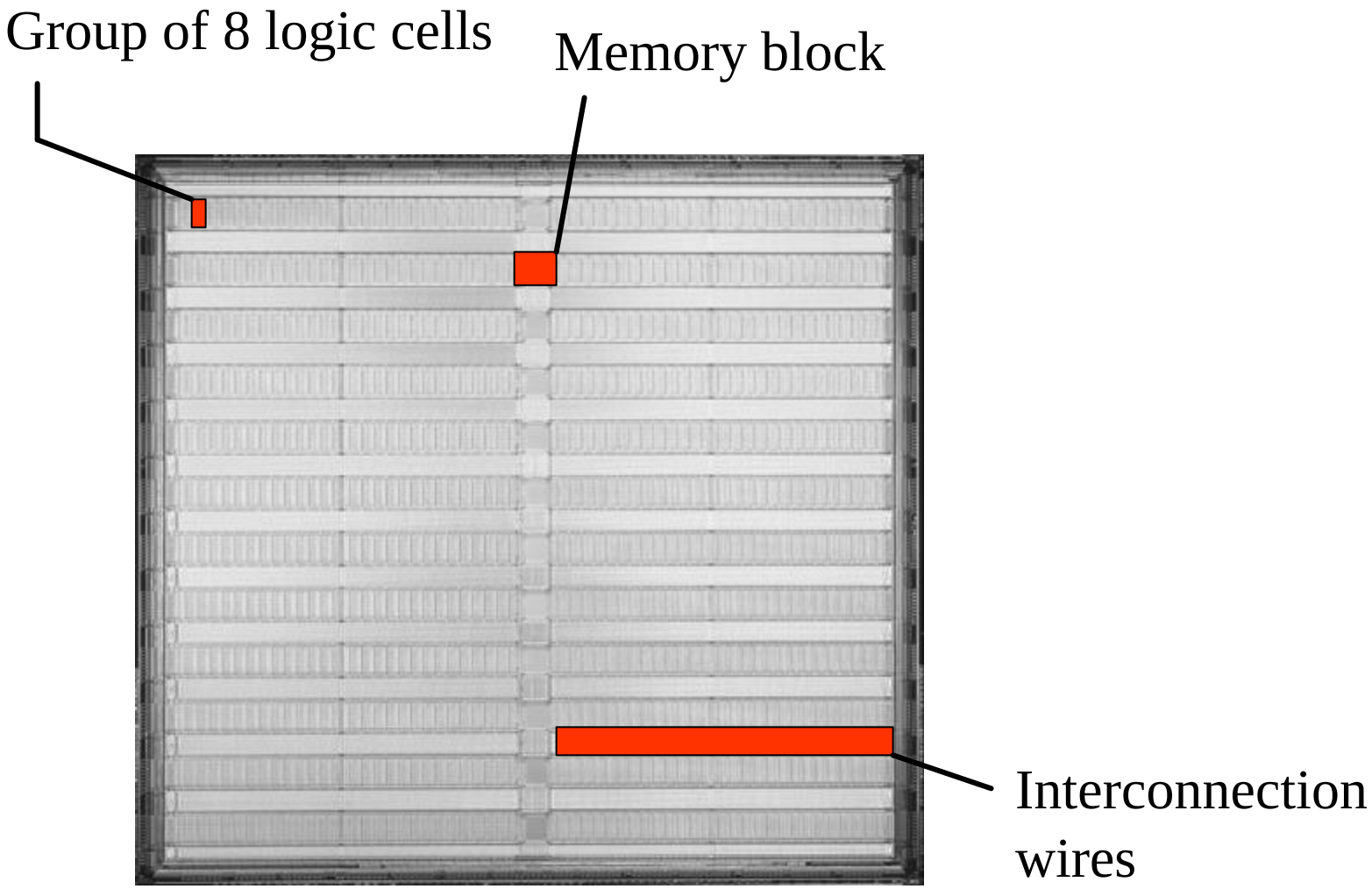

Figure 1.2 A field-programmable gate array chip

Please see “portrait orientation” PowerPoint file for Chapter 1

Figure 1.3 The development process

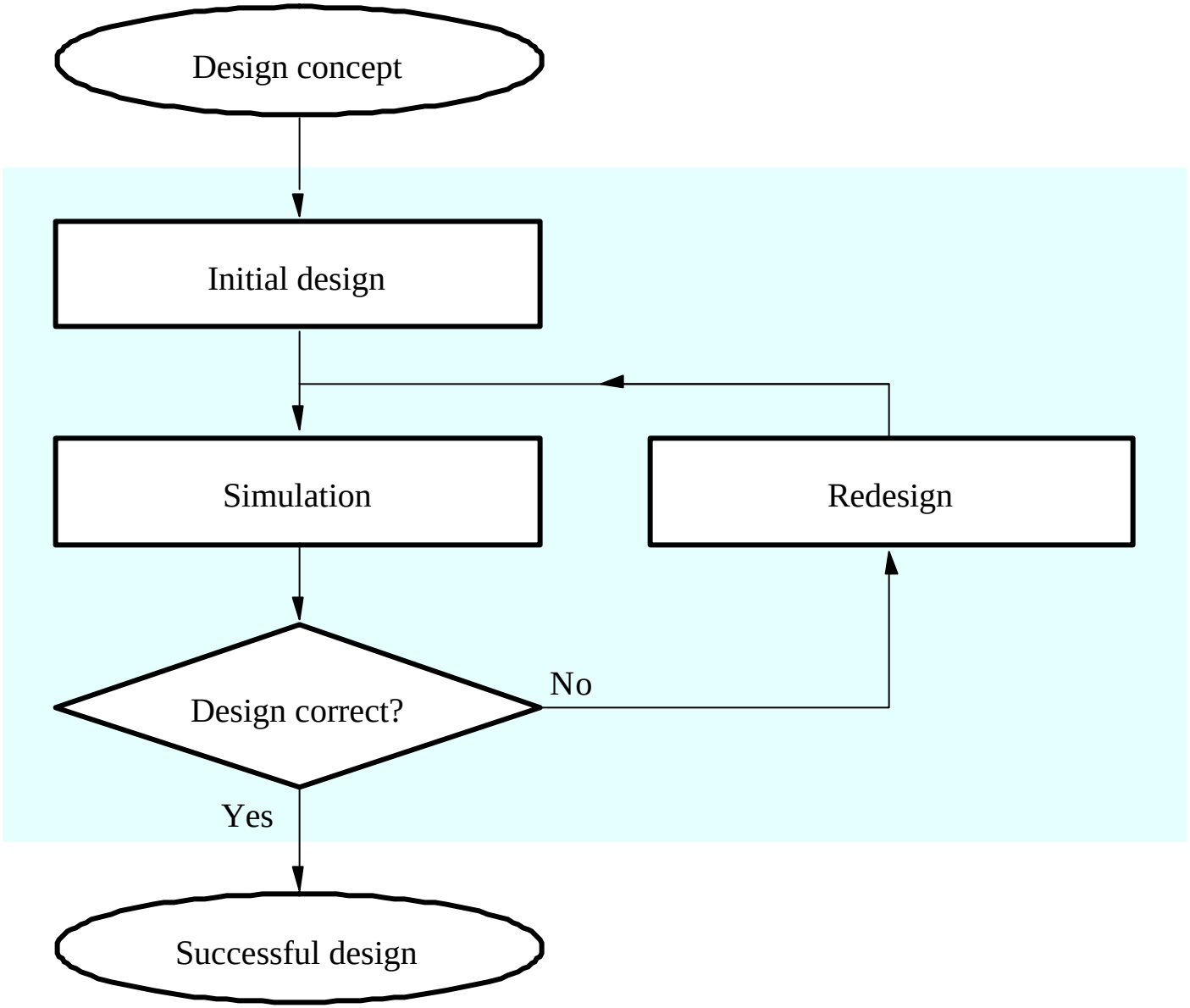

Figure 1.4 The basic design loop

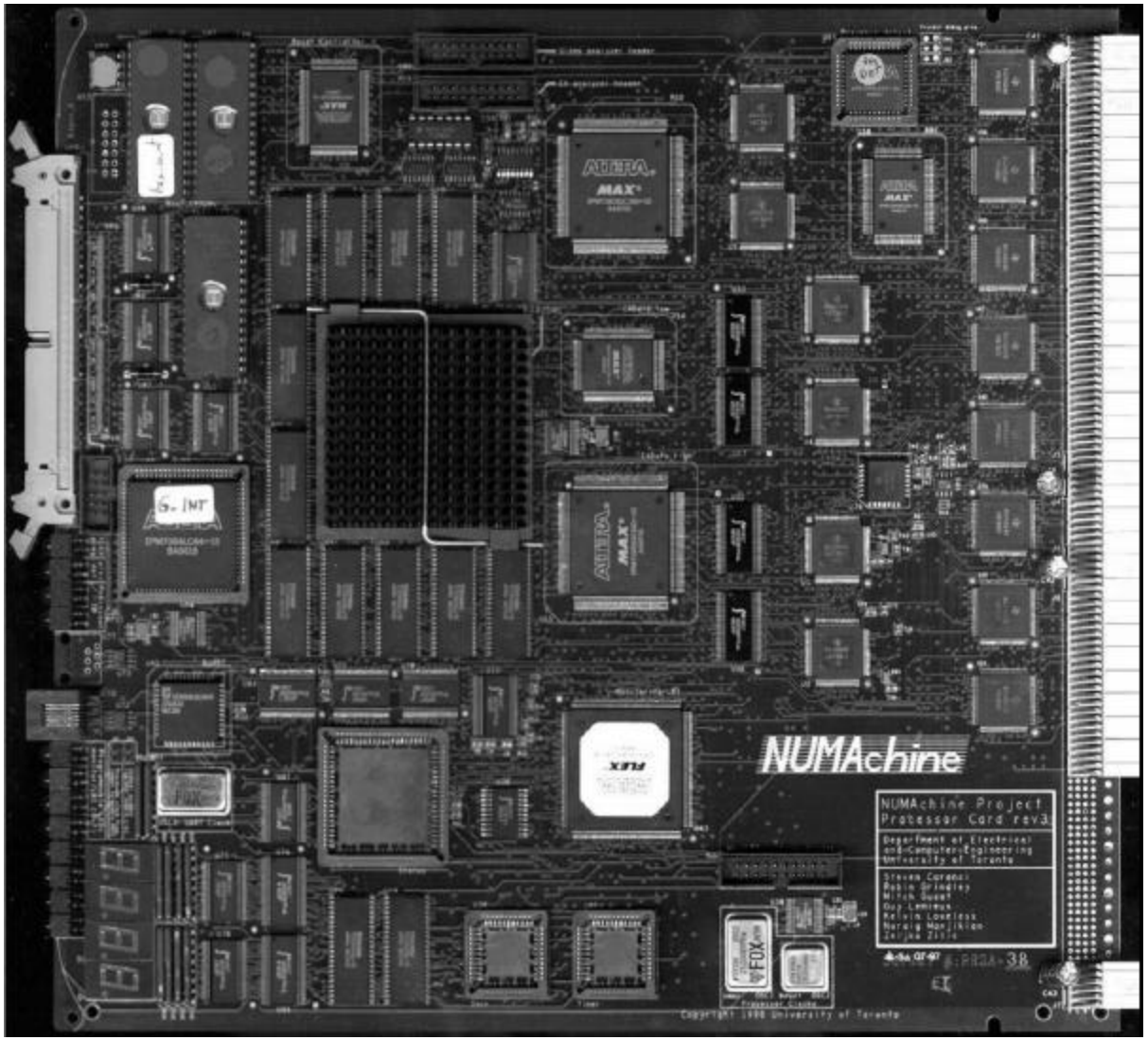

Figure 1.5 A printed circuit board

Please see “portrait orientation” PowerPoint file for Chapter 1

Figure 1.6 Design flow for logic circuits

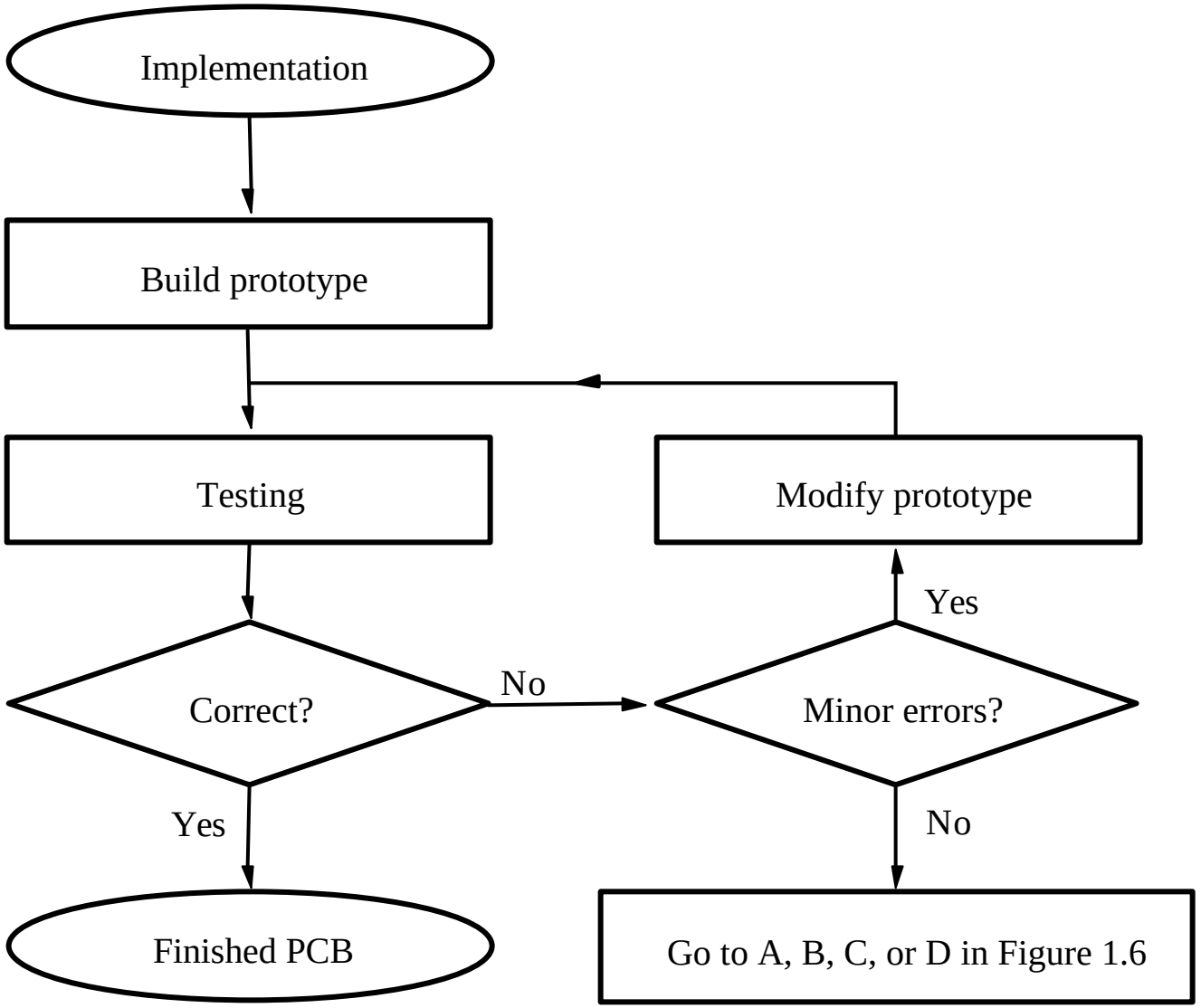

Figure 1.7 Completion of PCB development

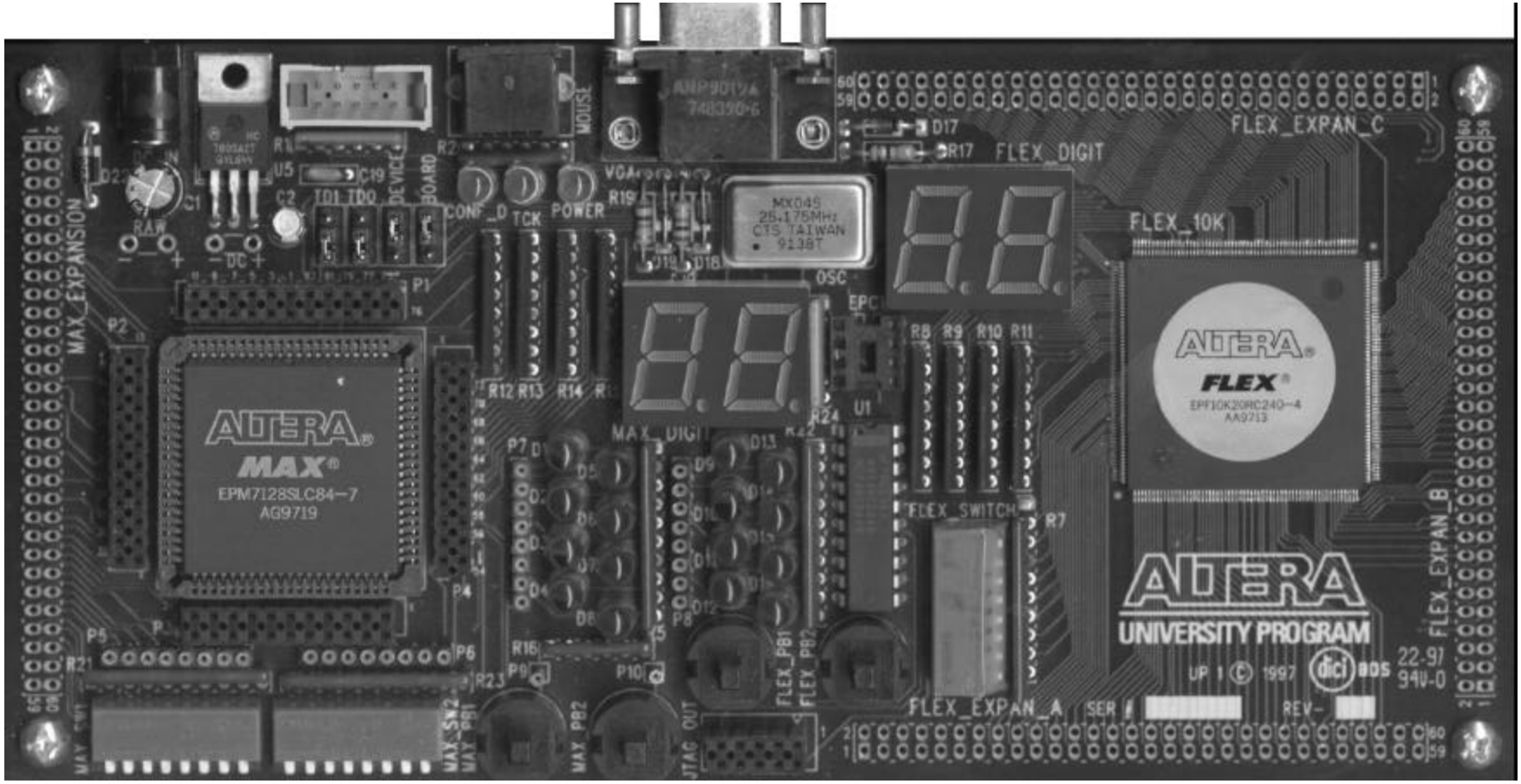

Figure 1.8 The Altera UP-1 Development Board