Voltage

V_{DD}

Logic value 1

$V_{1,min}$

Undefined

$V_{0,max}$

Logic value 0

V_{SS} (Gnd)

Figure 3.1 Logic values as voltage levels

$x = \text{"low"}$ $x = \text{"high"}$
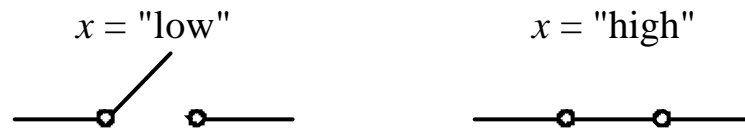
(a) A simple switch controlled by the input x

Gate

Source — — *Drain*

Substrate (Body)

(b) NMOS transistor

V_G

V_S — — V_D
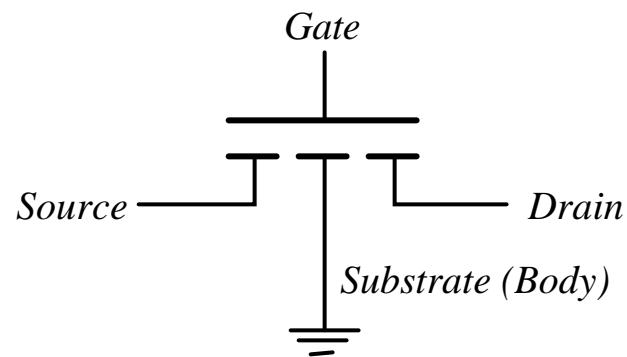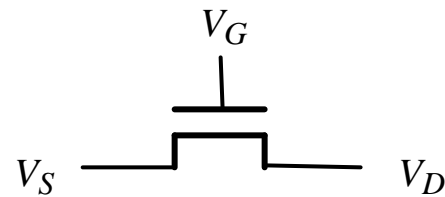
(c) Simplified symbol for an NMOS transistor

Figure 3.2   NMOS transistor as a switch

$x =$ "high"

$x =$ "low"
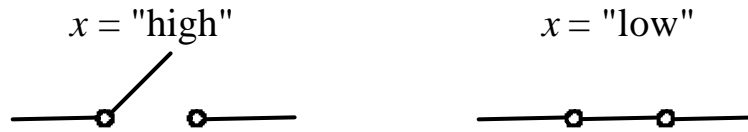
(a) A switch with the opposite behavior of Figure 3.2 *a*

Gate

Drain

Source

V_{DD}

Substrate (Body)

(b) PMOS transistor

V_G

V_S

V_D
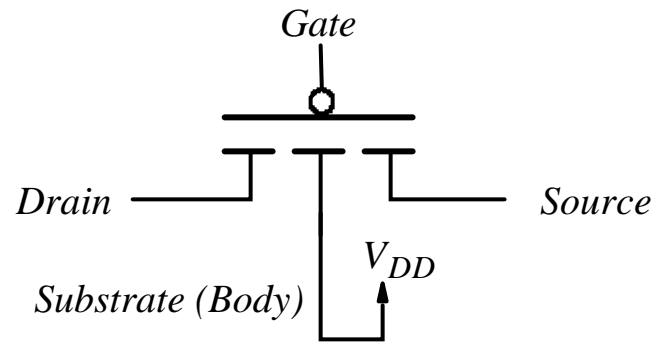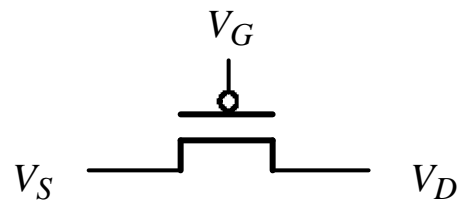
(c) Simplified symbol for an PMOS transistor

Figure 3.3   PMOS transistor as a switch

V_D

V_G

$V_S = 0 \text{ V}$

$V_D = 0 \text{ V}$

Closed switch
when $V_G = V_{DD}$

V_D

Open switch
when $V_G = 0 \text{ V}$

(a) NMOS transistor

$V_S = V_{DD}$

V_G

V_D

V_{DD}

V_D

Open switch
when $V_G = V_{DD}$

V_{DD}

$V_D = V_{DD}$

Closed switch
when $V_G = 0 \text{ V}$
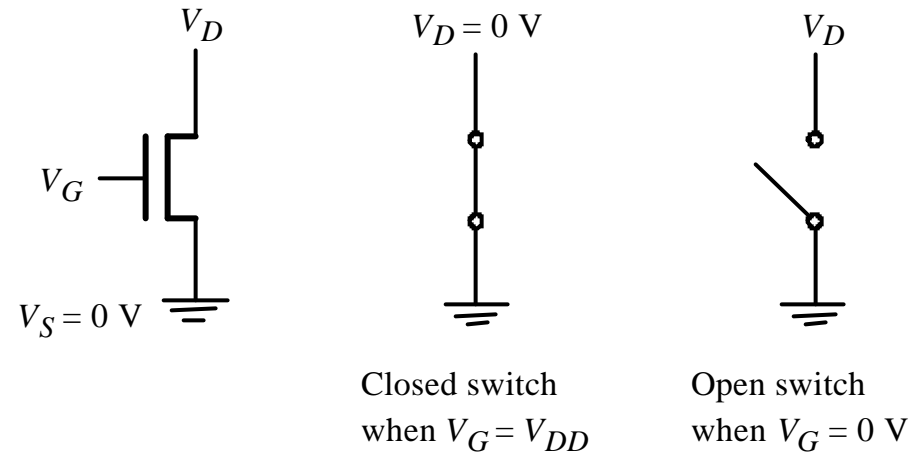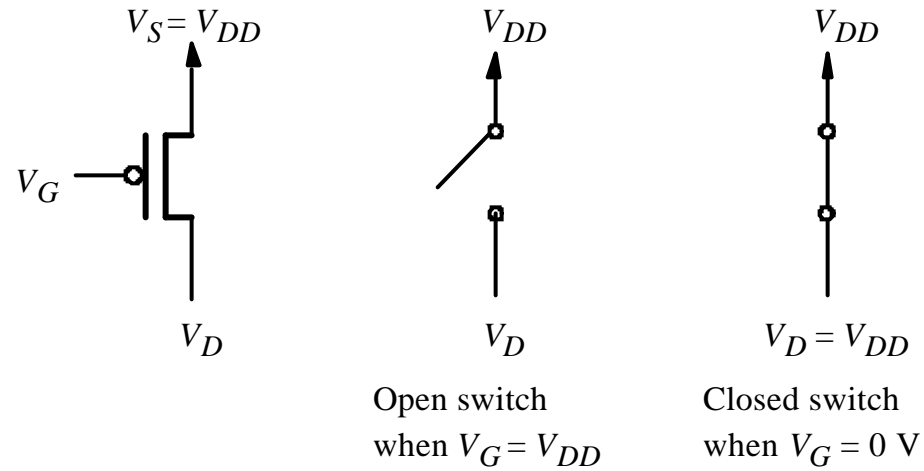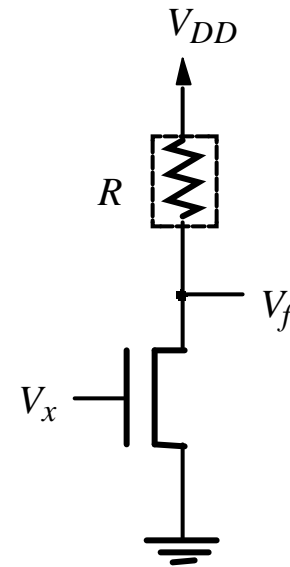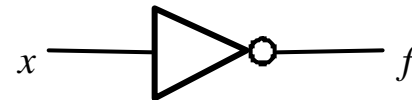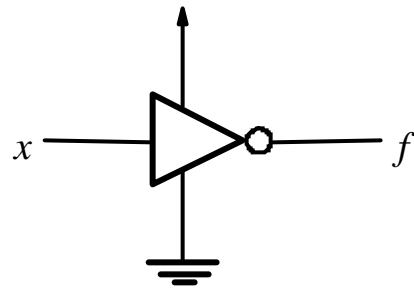
(b) PMOS transistor

Figure 3.4   NMOS and PMOS transistors in logic circuits
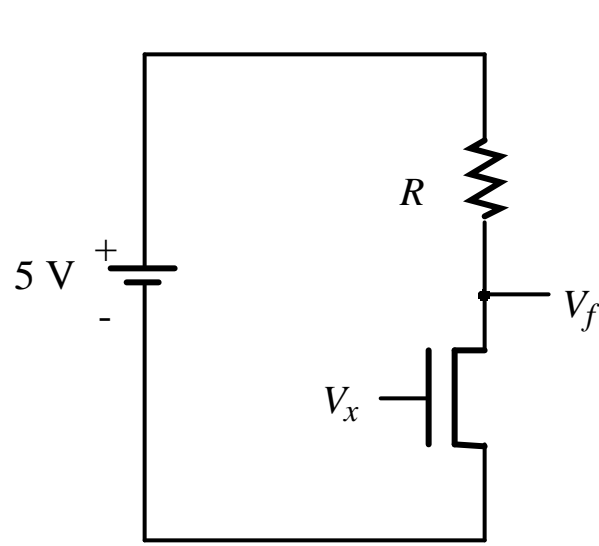
(a) Circuit diagram

(b) Simplified circuit diagram

(c) Graphical symbols

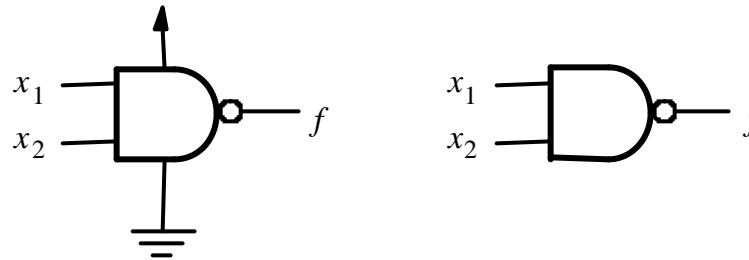Figure 3.5   A NOT gate built using NMOS technology

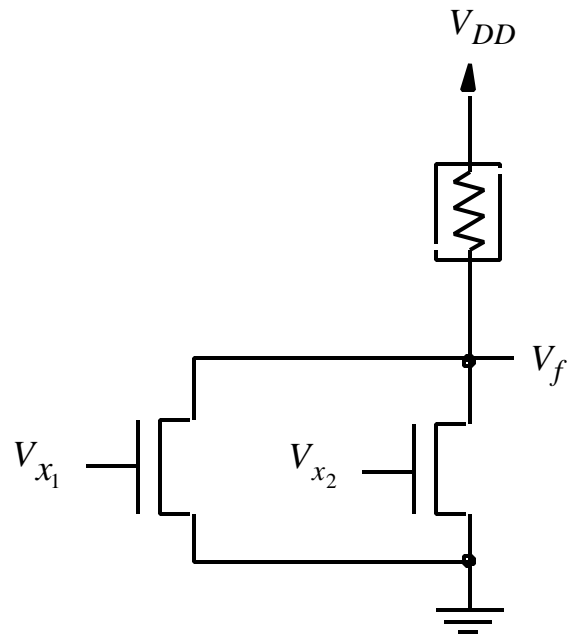| x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0

(a) Circuit   (b) Truth table

(c) Graphical symbols

Figure 3.6   NMOS realization of a NAND gate

(a) Circuit

x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	0

(b) Truth table
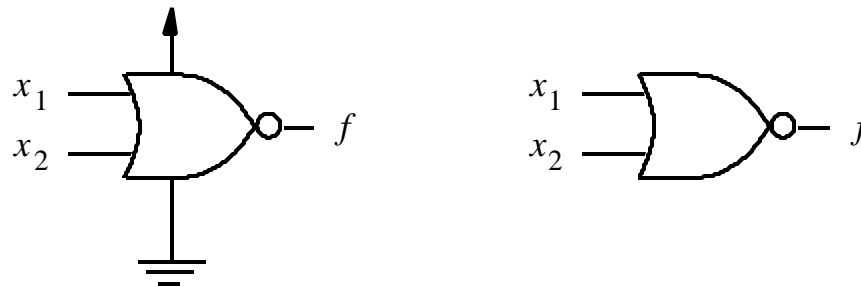
(c) Graphical symbols

Figure 3.7   NMOS realization of a NOR gate

x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1

(a) Circuit

(b) Truth table

(c) Graphical symbols

Figure 3.8   NMOS realization of an AND gate

(a) Circuit

x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	1

(b) Truth table

(c) Graphical symbols
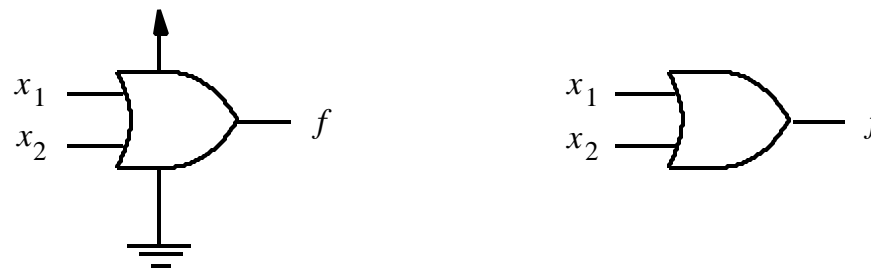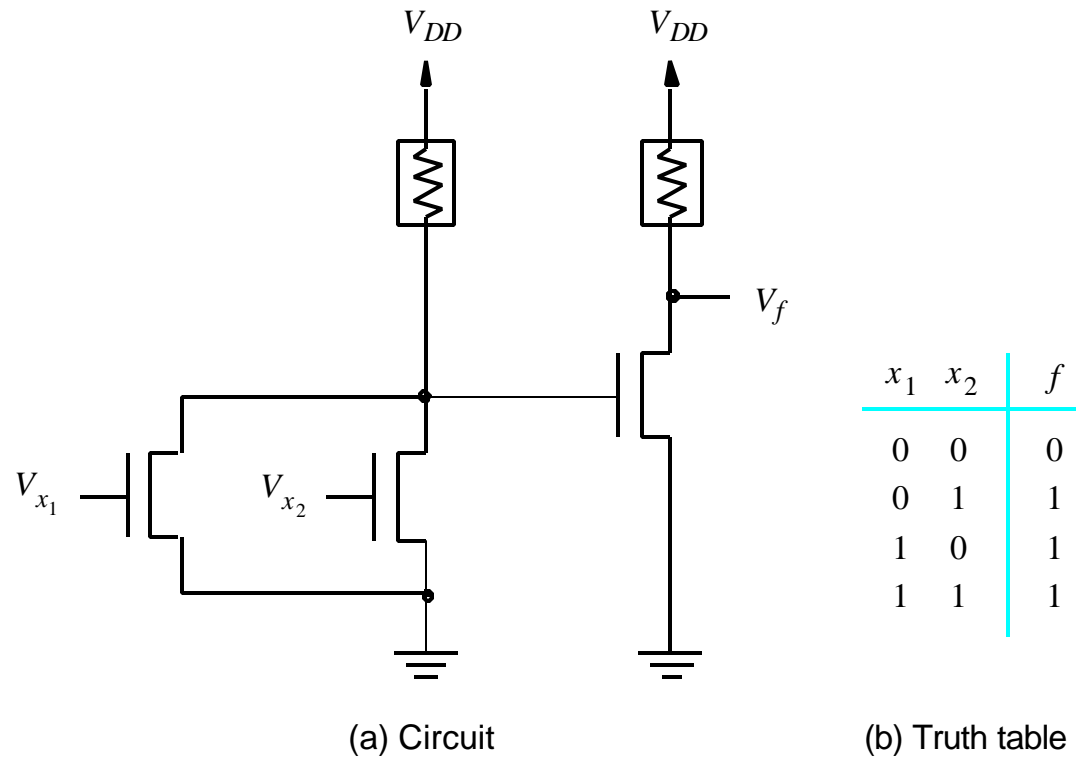
Figure 3.9 NMOS realization of an OR gate

V_{DD}

V_f

V_{x_1}

V_{x_n}
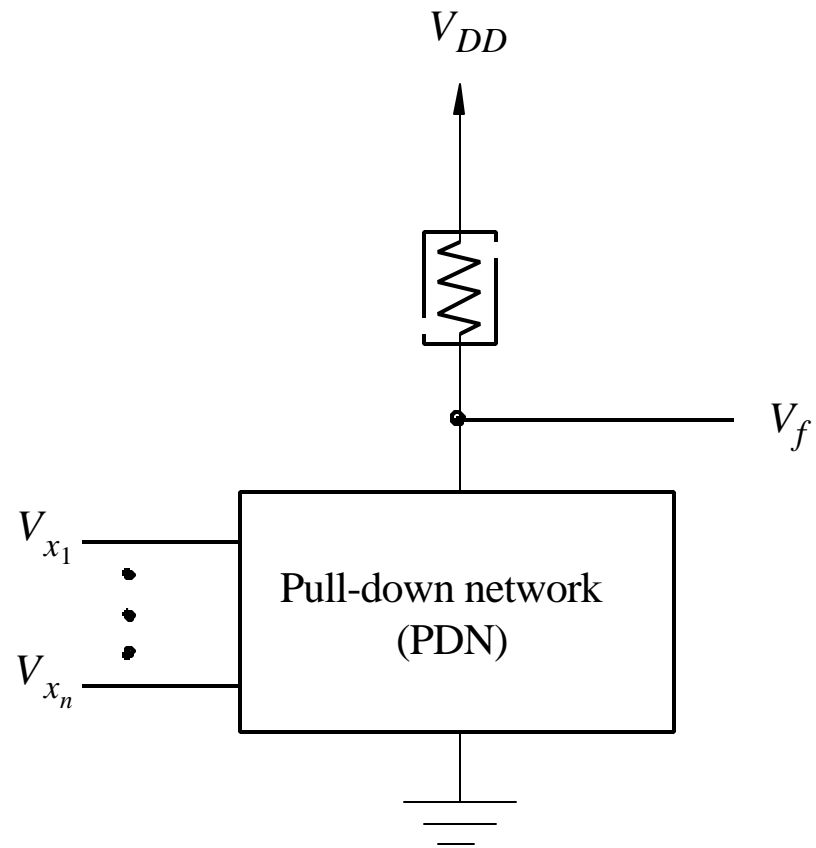
Pull-down network
(PDN)

Figure 3.10   Structure of an NMOS circuit
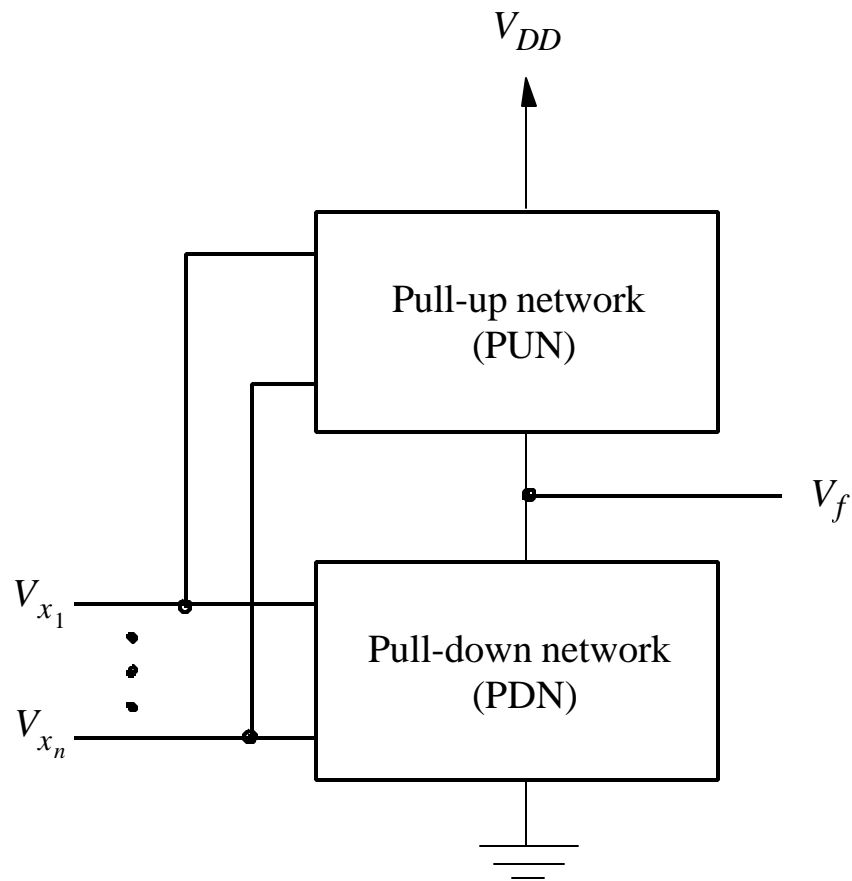
Figure 3.11   Structure of a CMOS circuit
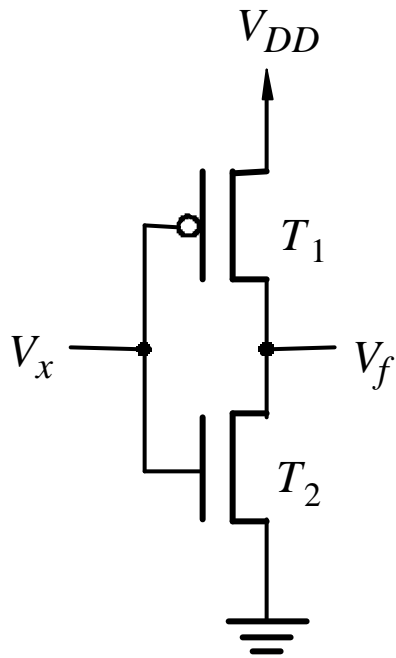
x	T_1	T_2	f
0	on	off	1
1	off	on	0

(a) Circuit   (b) Truth table and transistor states

Figure 3.12   CMOS realization of a NOT gate
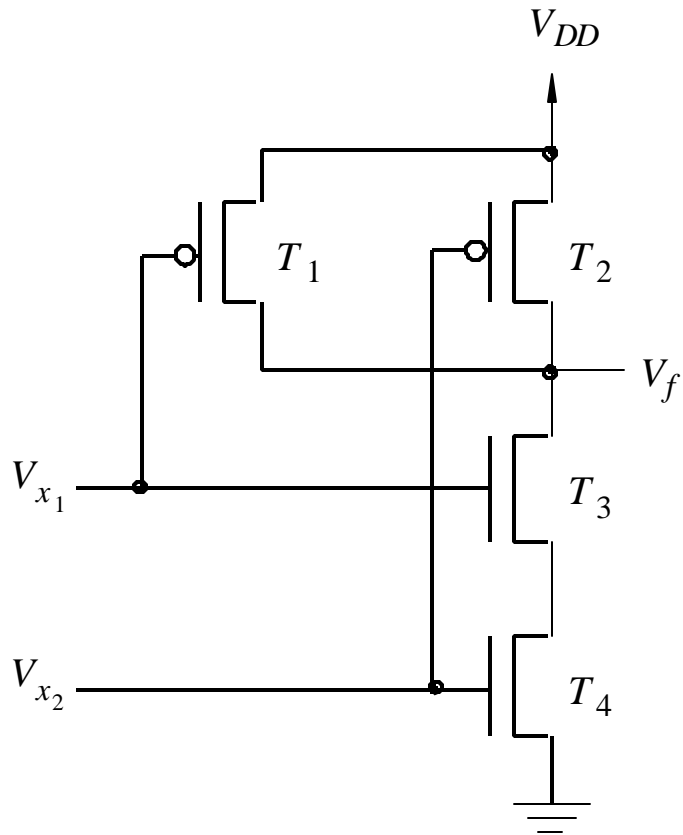
x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

(a) Circuit　　　　　　(b) Truth table and transistor states

Figure 3.13　CMOS realization of a NAND gate
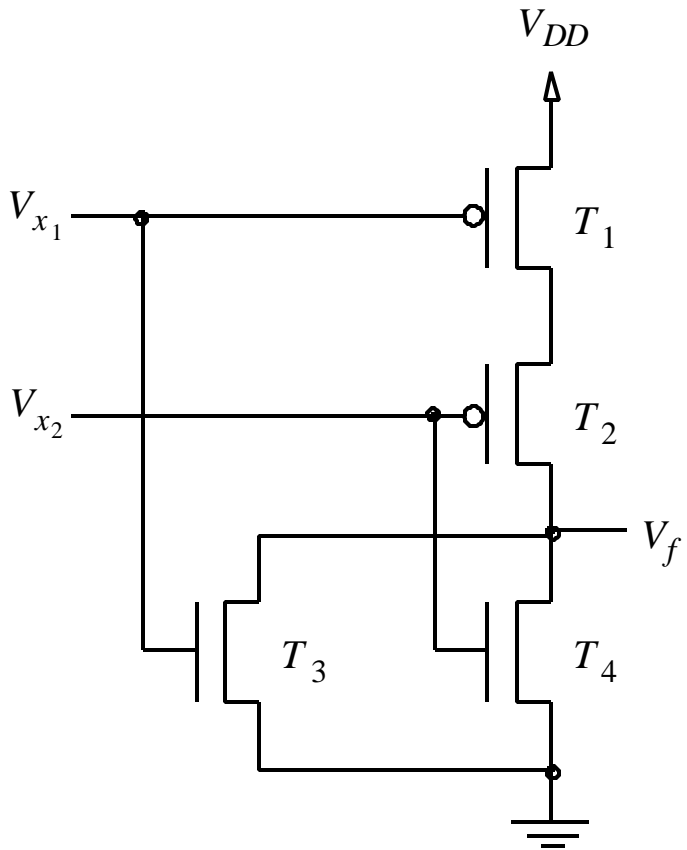
x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

(a) Circuit   (b) Truth table and transistor states

Figure 3.14   CMOS realization of a NOR gate
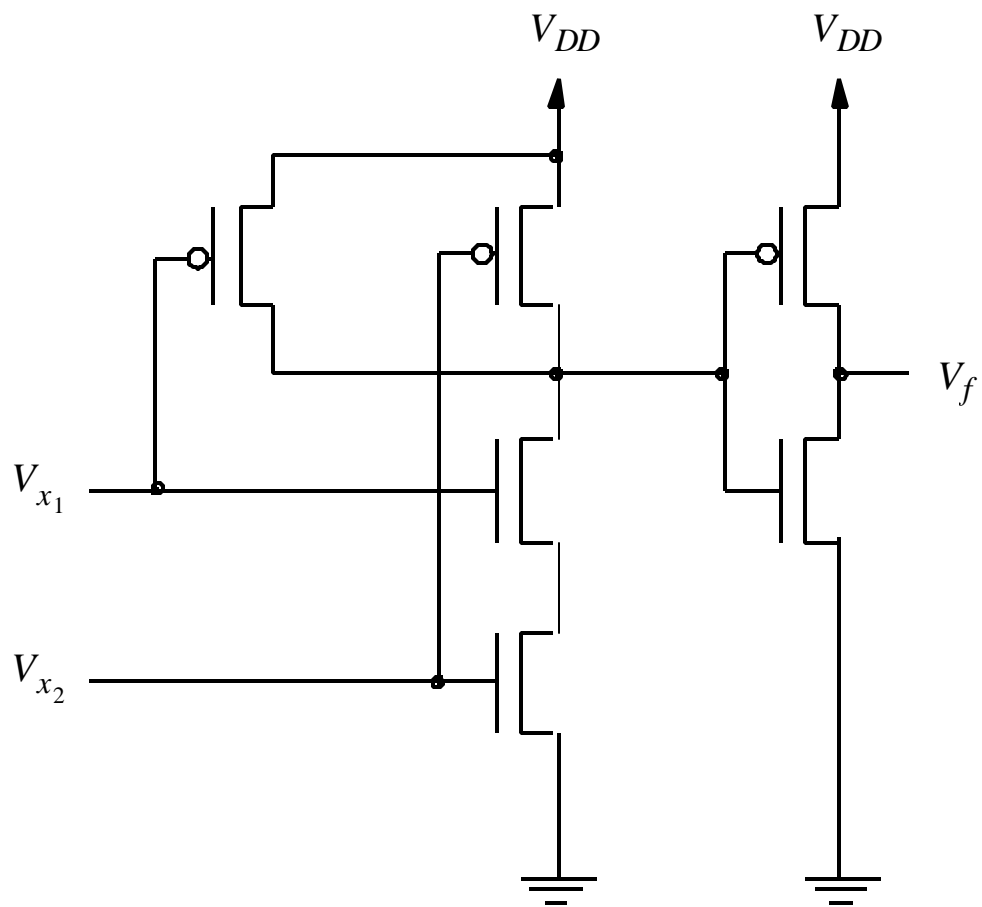
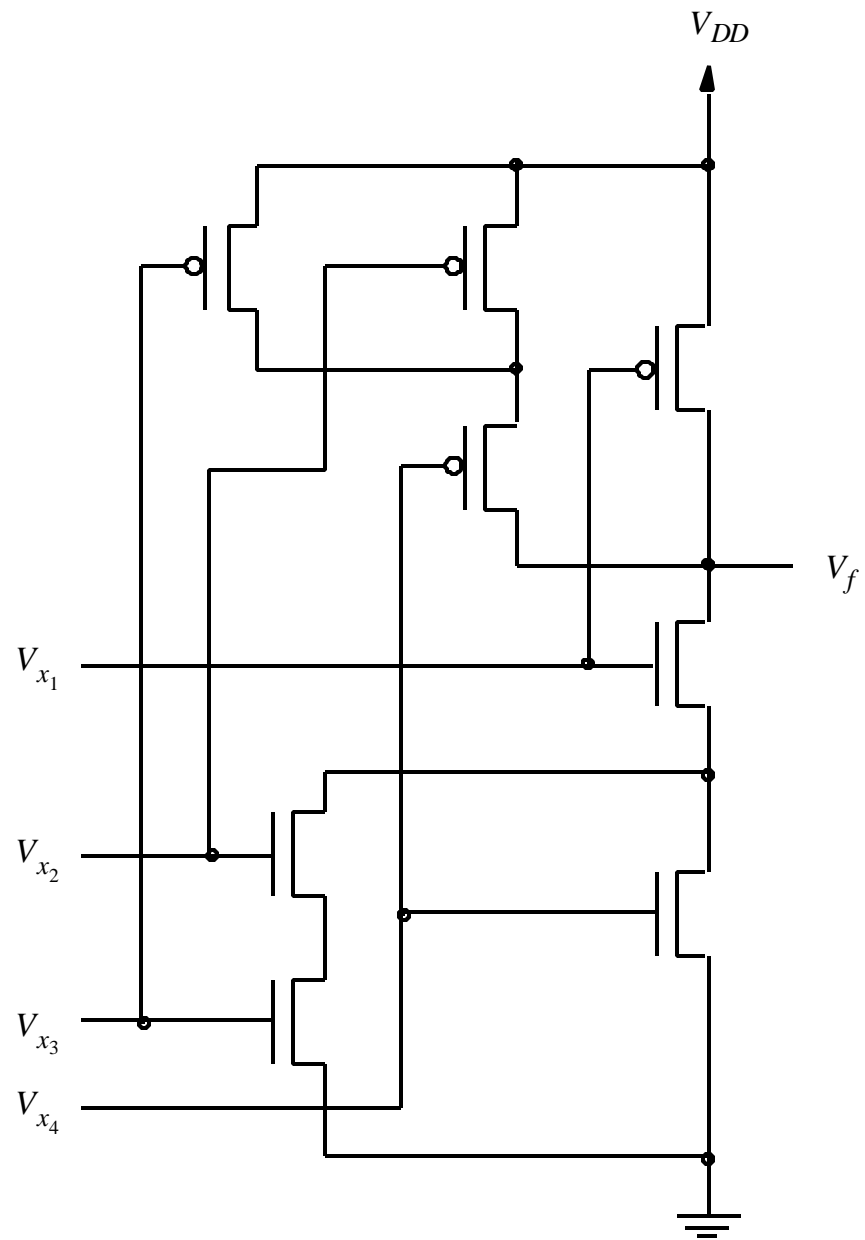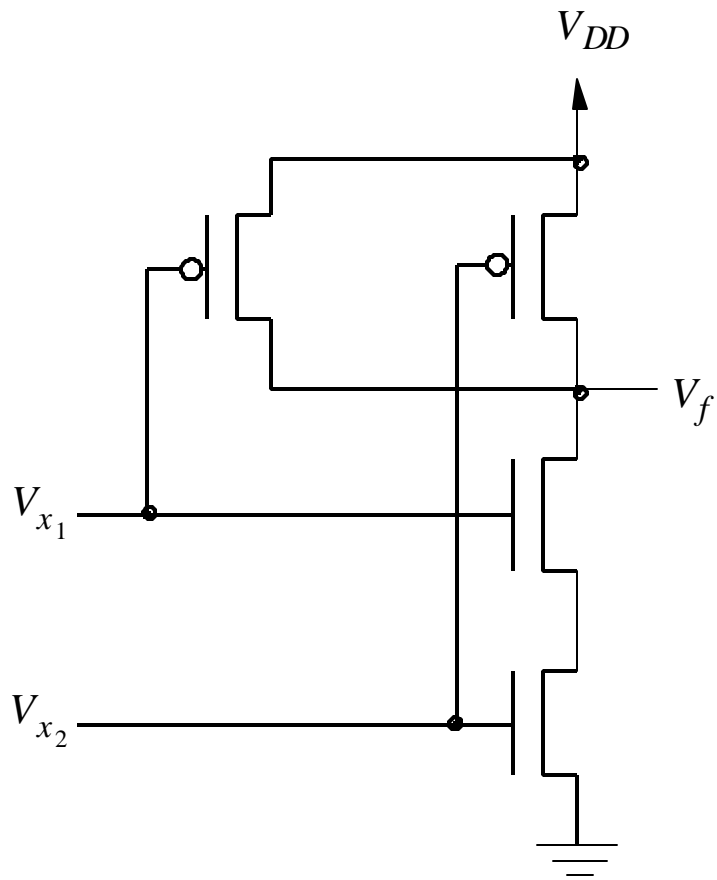Figure 3.15   CMOS realization of an AND gate
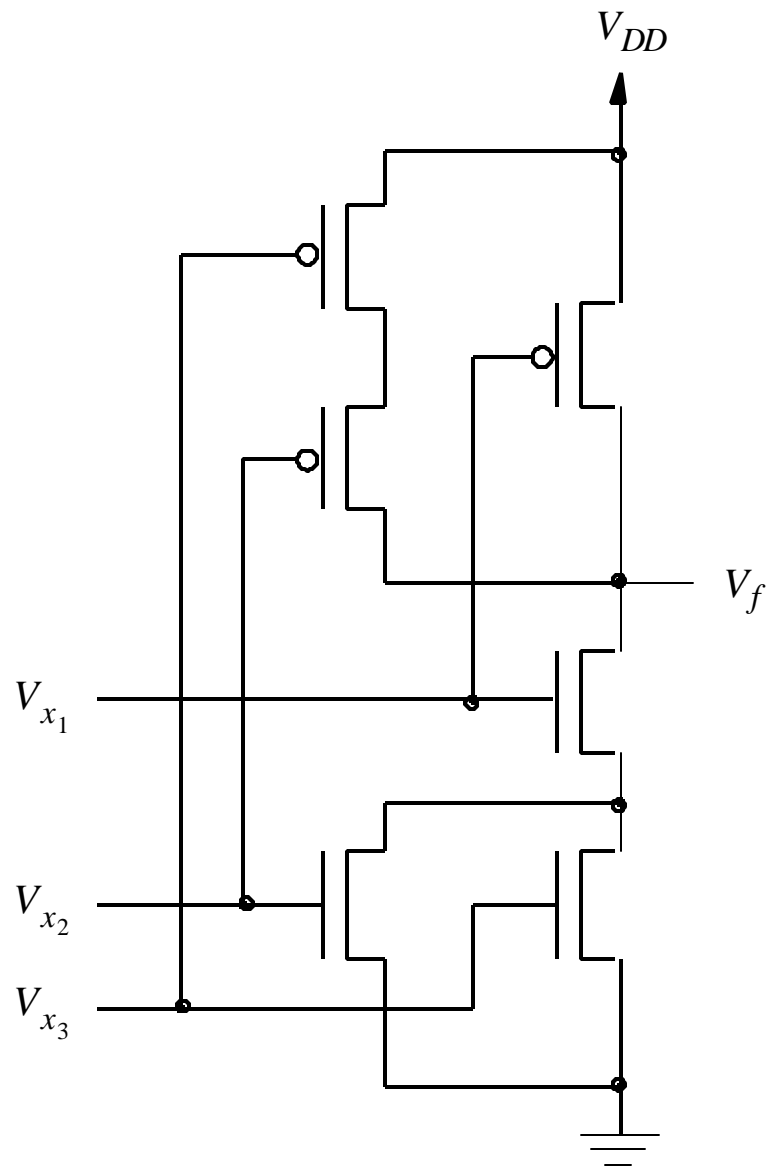
Figure 3.16   A CMOS complex gate

Figure 3.17   A CMOS complex gate

	V_{x_1}	V_{x_2}	V_f
	L	L	H
	L	H	H
	H	L	H
	H	H	L

(a) Circuit

(b) Voltage levels

Figure 3.18   Voltage levels in a CMOS circuit

$$\begin{array}{cc|c} x_1 & x_2 & f \\ \hline 0 & 0 & 1 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{array}$$

V_{x_1}	V_{x_2}	V_f
L	L	H
L	H	H
H	L	H
H	H	L

(b) Positive logic truth table and gate symbol

(a) Voltage levels
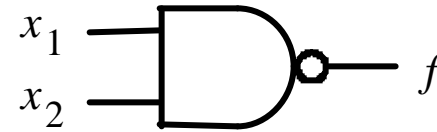
$$\begin{array}{cc|c} x_1 & x_2 & f \\ \hline 1 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{array}$$

(c) Negative logic truth table and gate symbol

Figure 3.19   Interpretation of voltage levels

x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1

(b) Positive logic

V_{x_1}	V_{x_2}	V_f
L	L	L
L	H	L
H	L	L
H	H	H
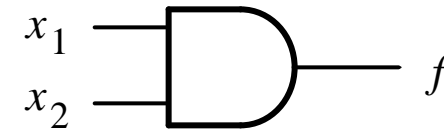
(a) Voltage levels

x_1	x_2	f
1	1	1
1	0	1
0	1	1
0	0	0

(c) Negative logic

Figure 3.20   Interpretation of voltage levels
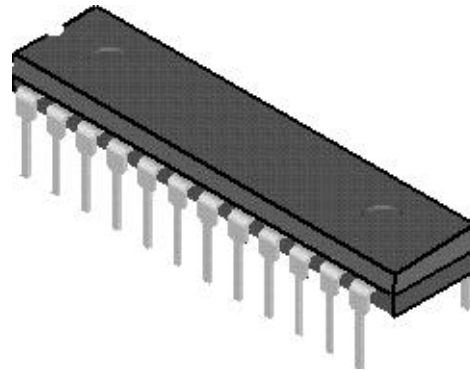
(a) Dual-inline package
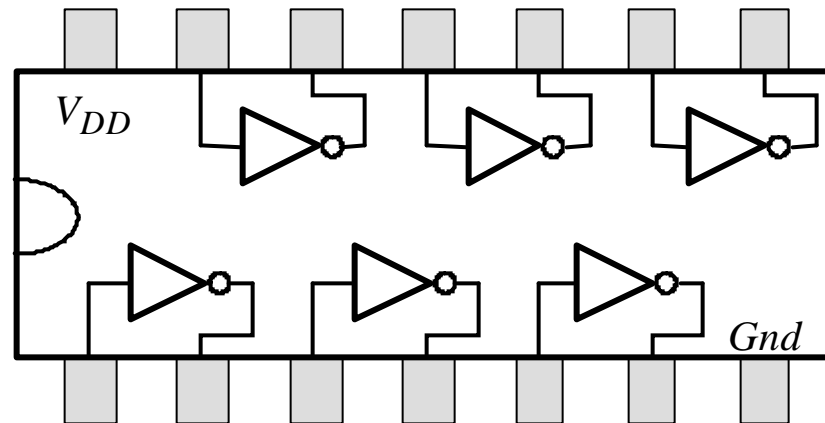
(b) Structure of 7404 chip

Figure 3.21   A 7400-series chip
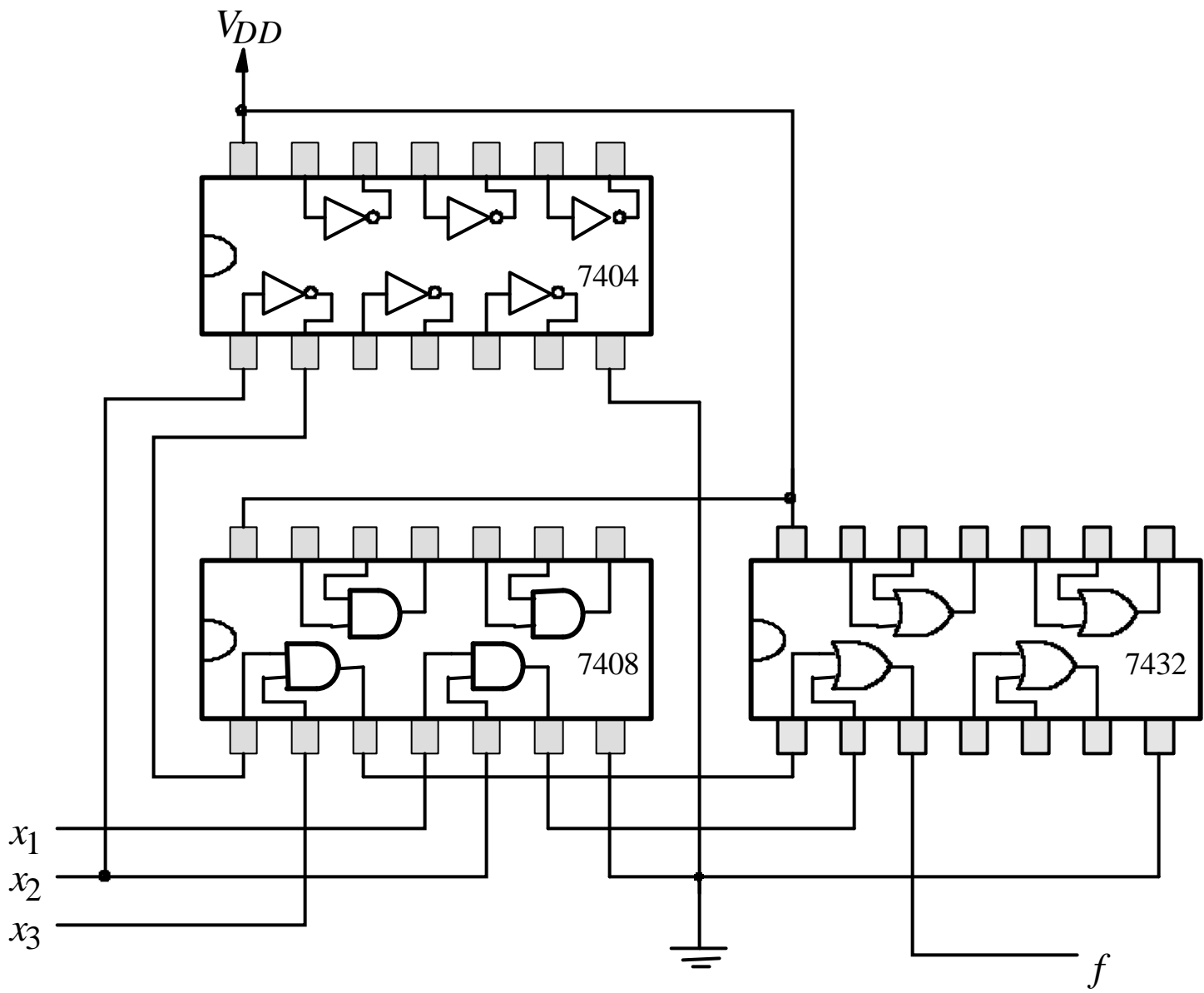
Figure 3.22   Implementation of $f = x_1\bar{x}_2 + x_2x_3$
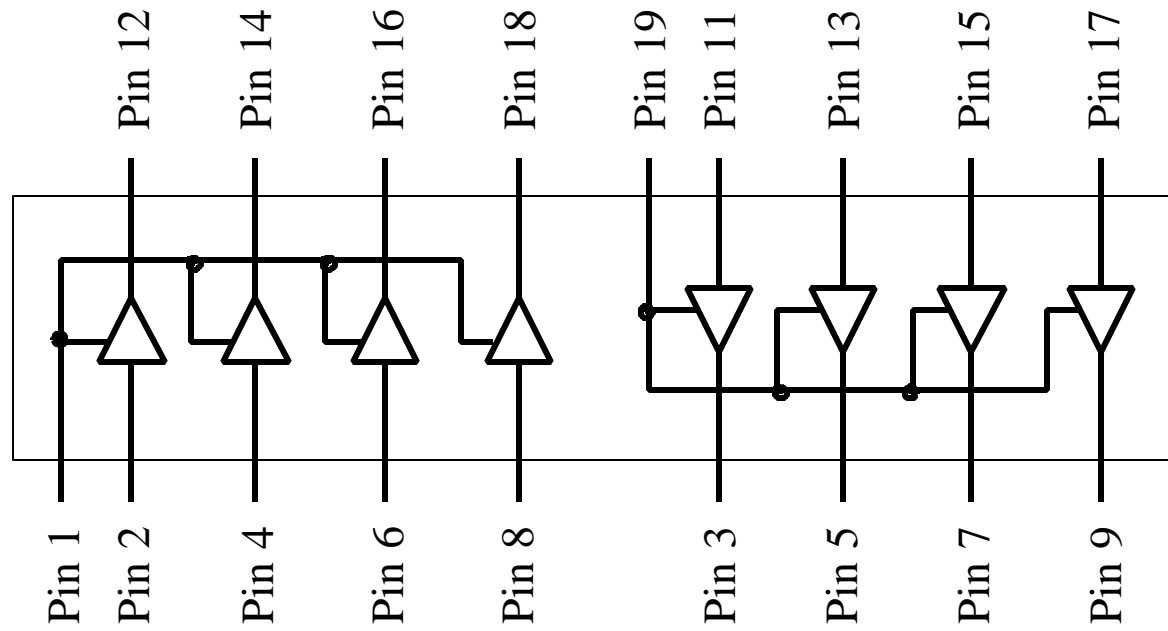
Figure 3.23   The 74244 buffer chip

Inputs

(logic variables)

**Logic gates
and
programmable
switches**

Outputs

(logic functions)
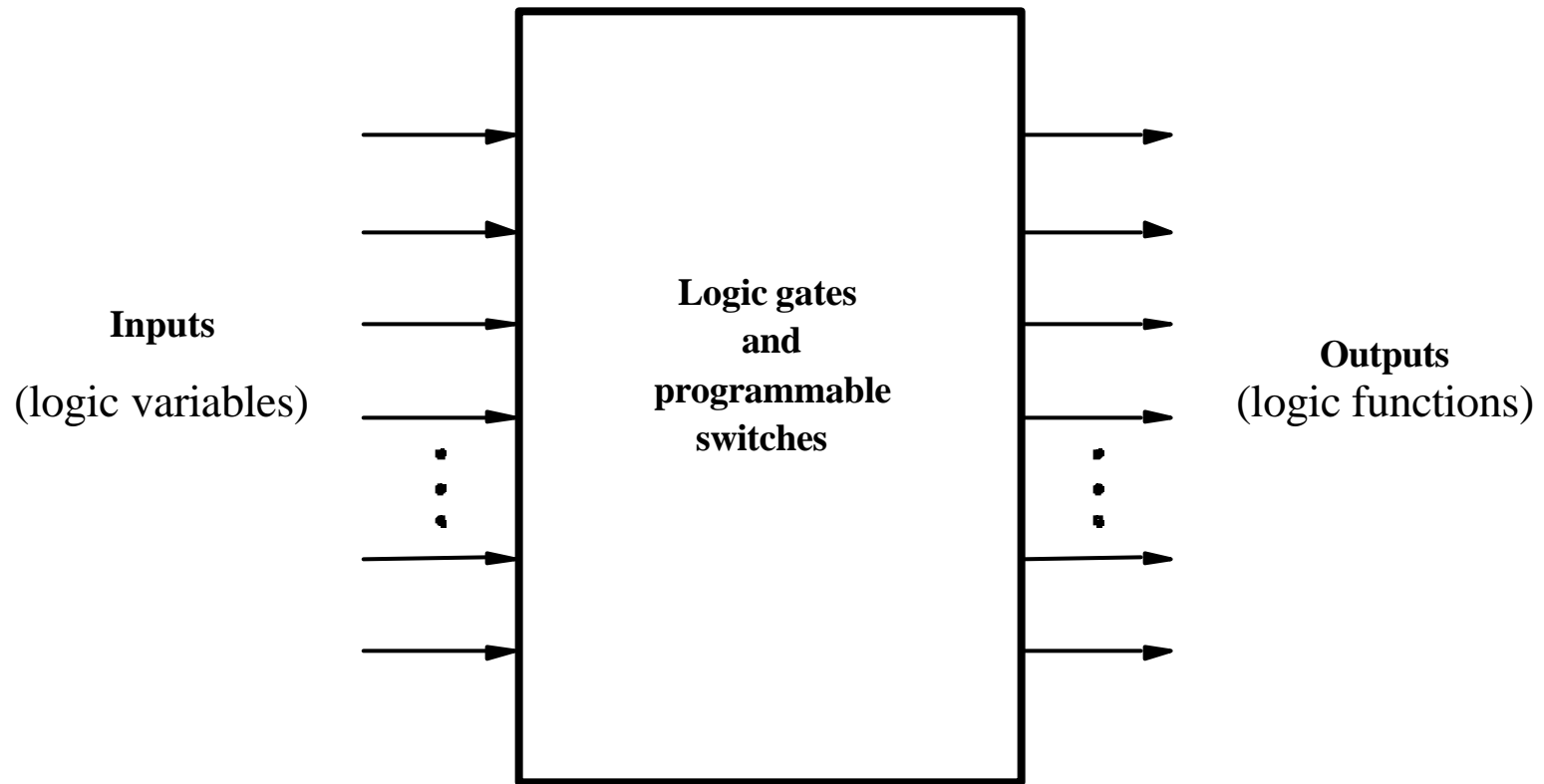
Figure 3.24   Programmable logic device as a black box
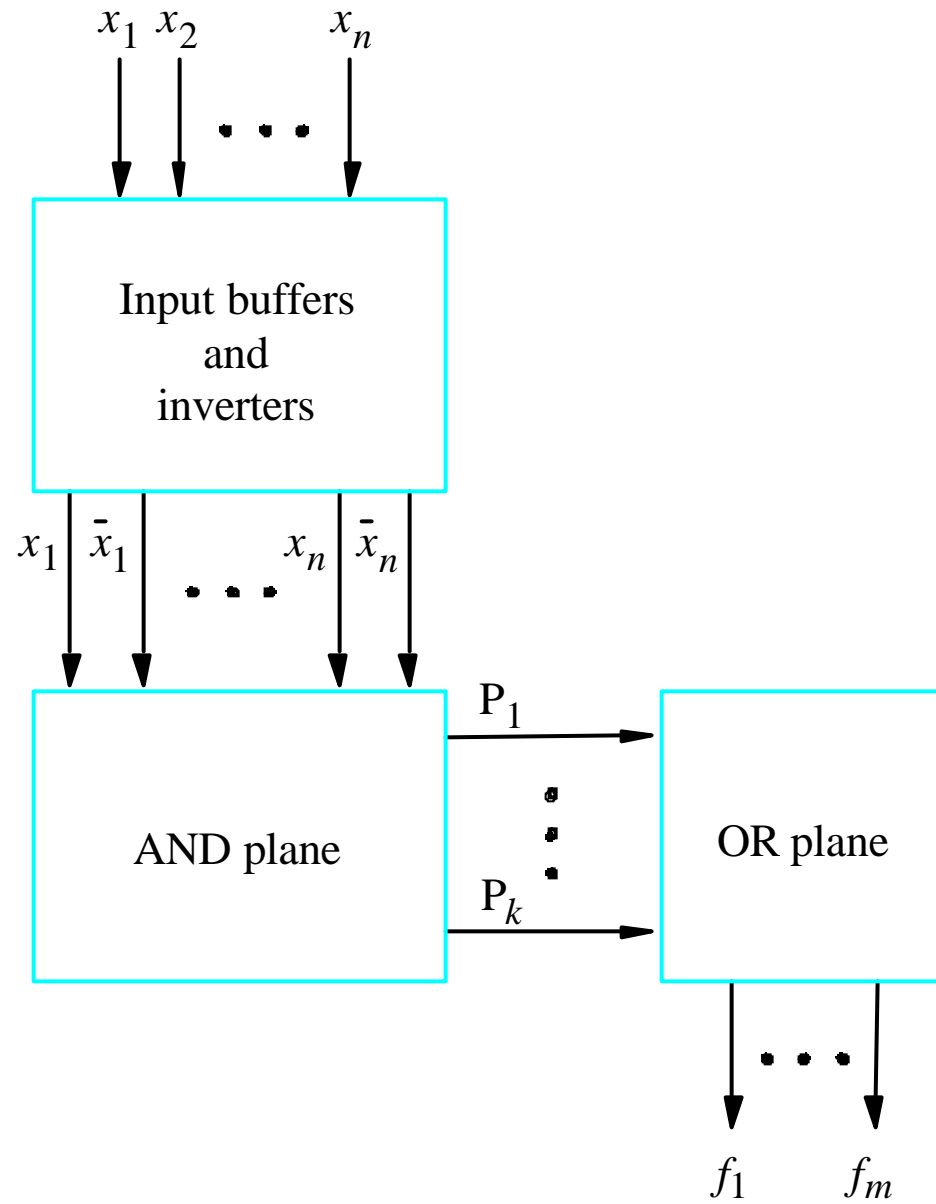
Figure 3.25   General structure of a PLA
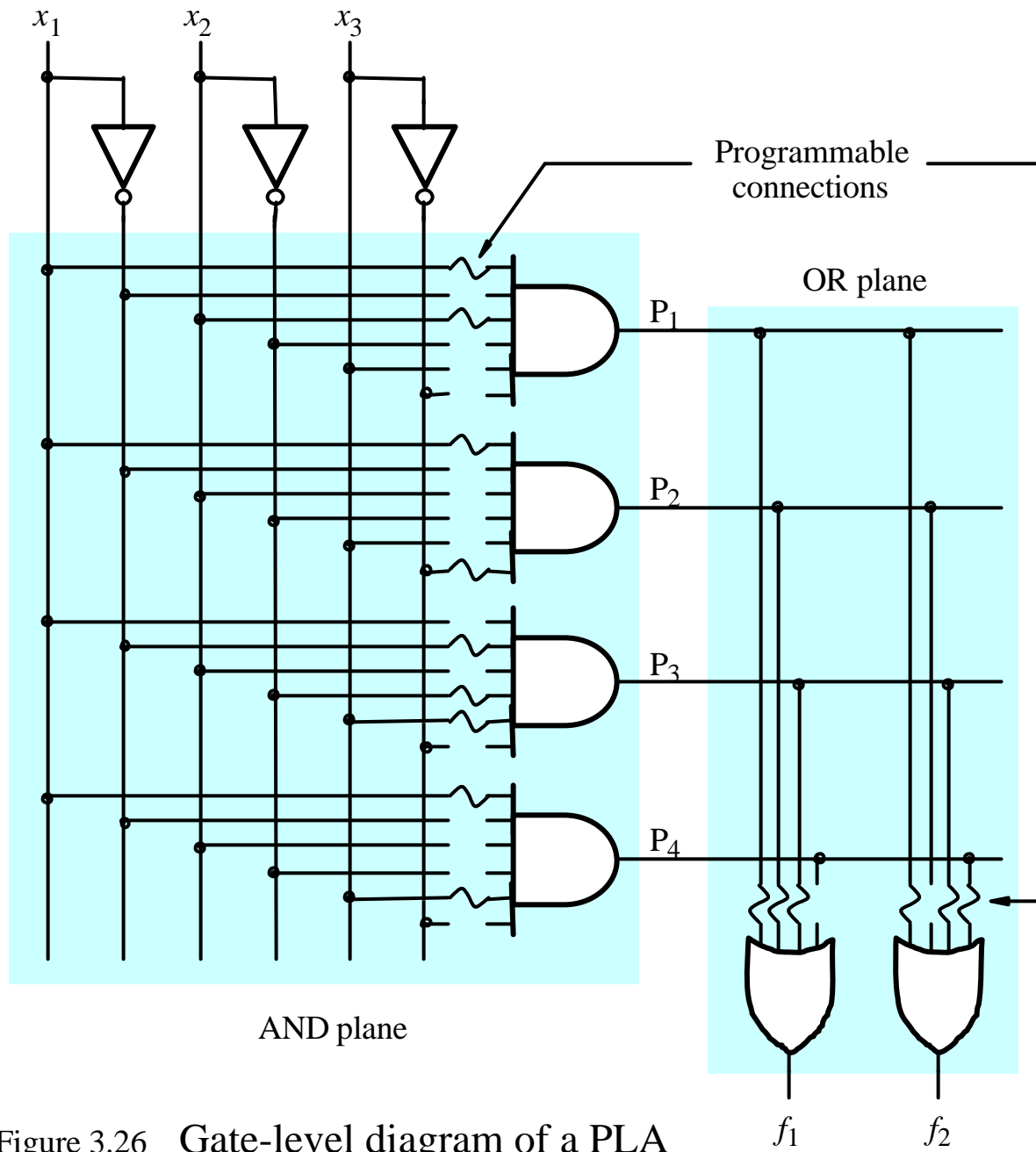
Figure 3.26   Gate-level diagram of a PLA
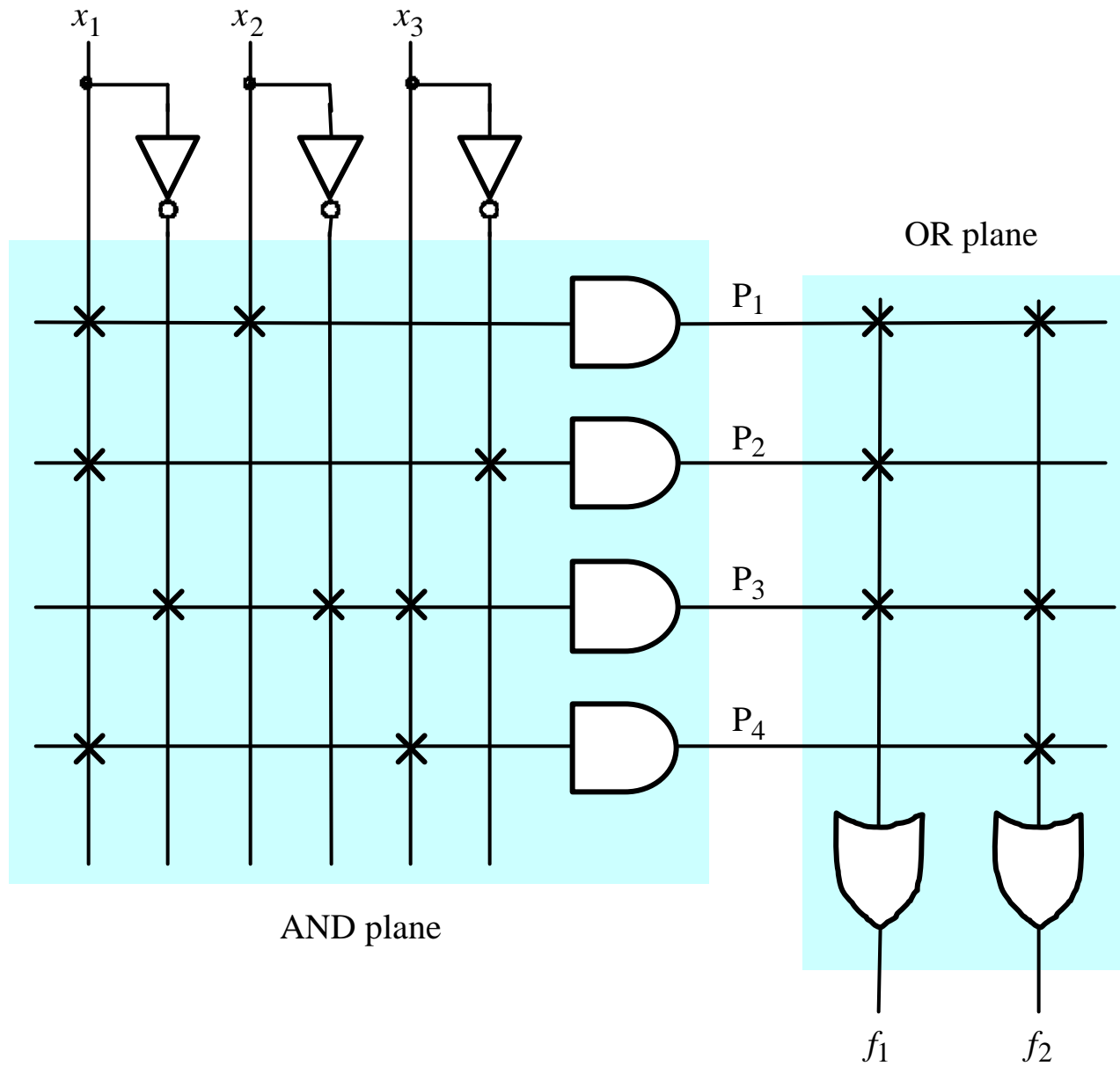
Figure 3.27   Customary schematic of a PLA
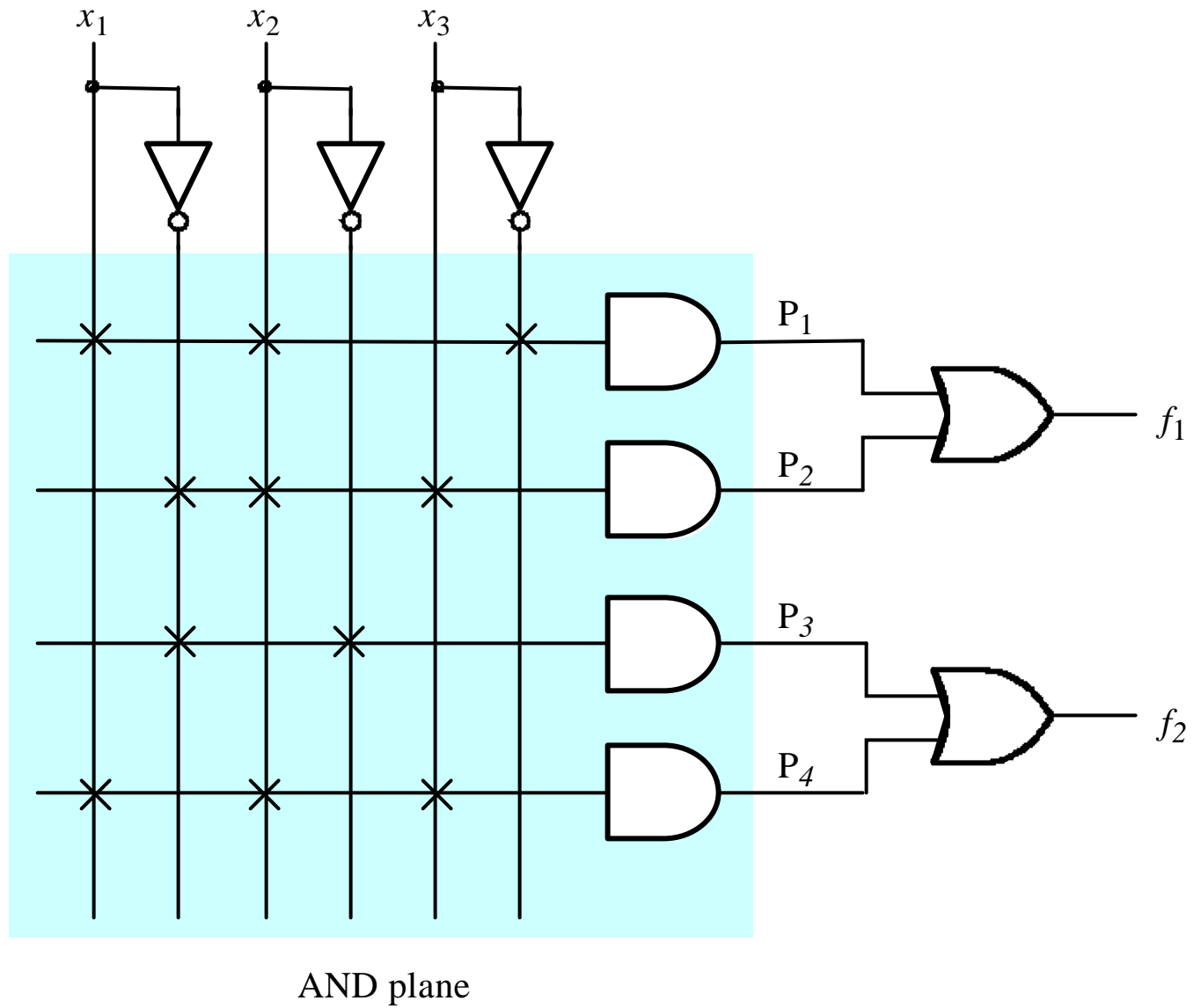
Figure 3.28   An example of a PLA

Select

Enable

Flip-flop

f_1

D   Q

Clock

To AND plane
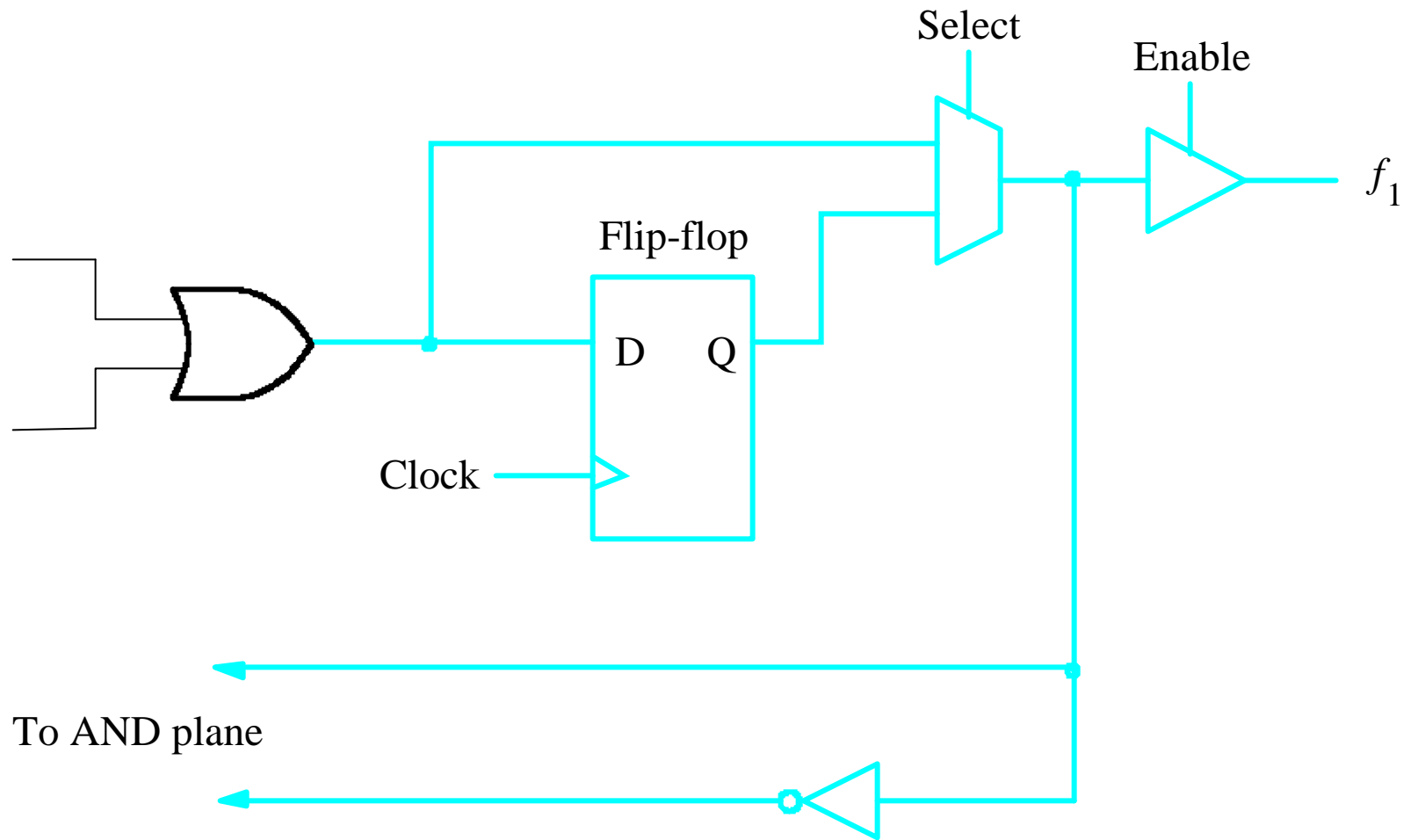
Figure 3.29   Output circuitry

Figure 3.30   A PLD programming unit

Printed circuit board
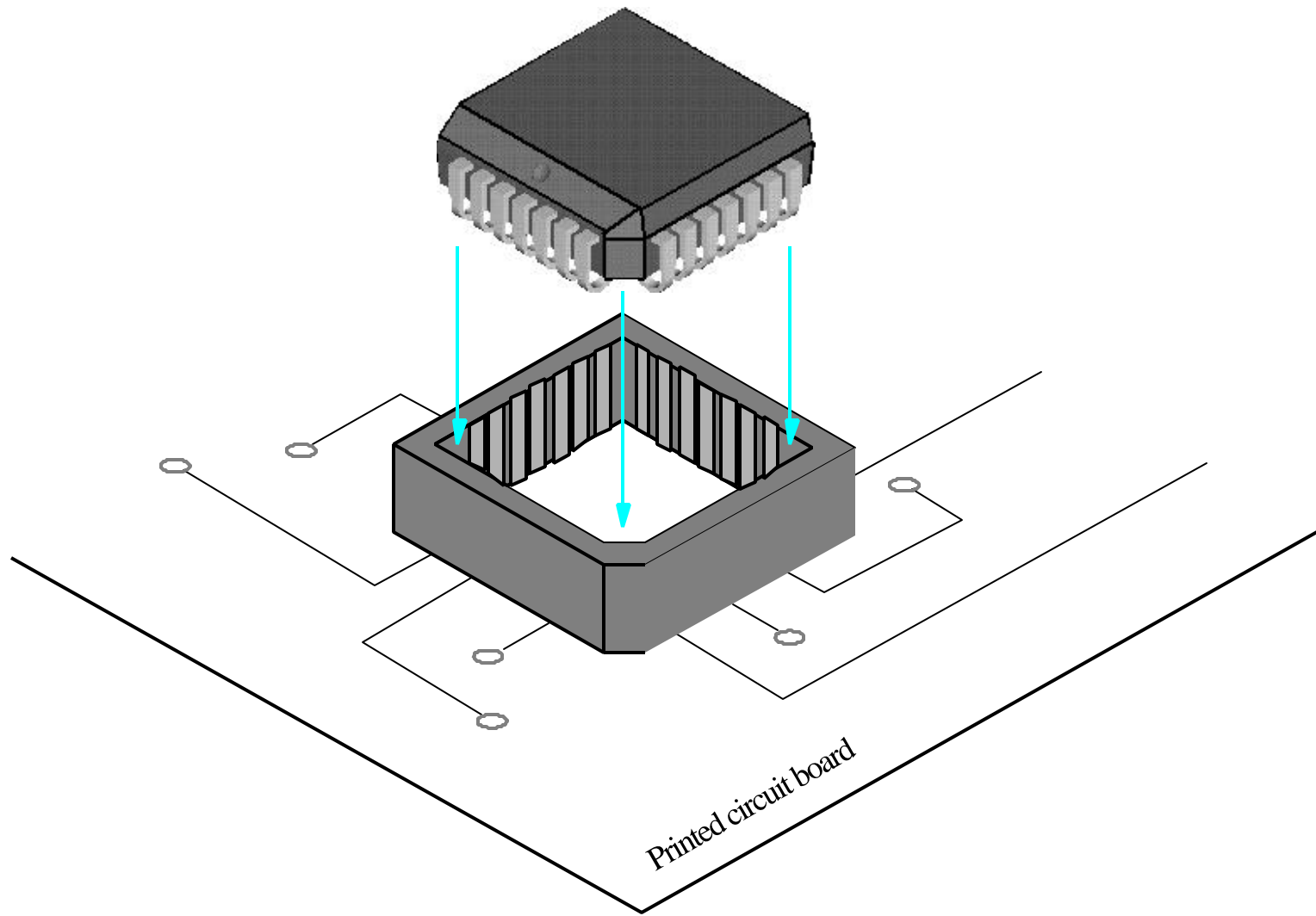
Figure 3.31   A PLCC package with socket
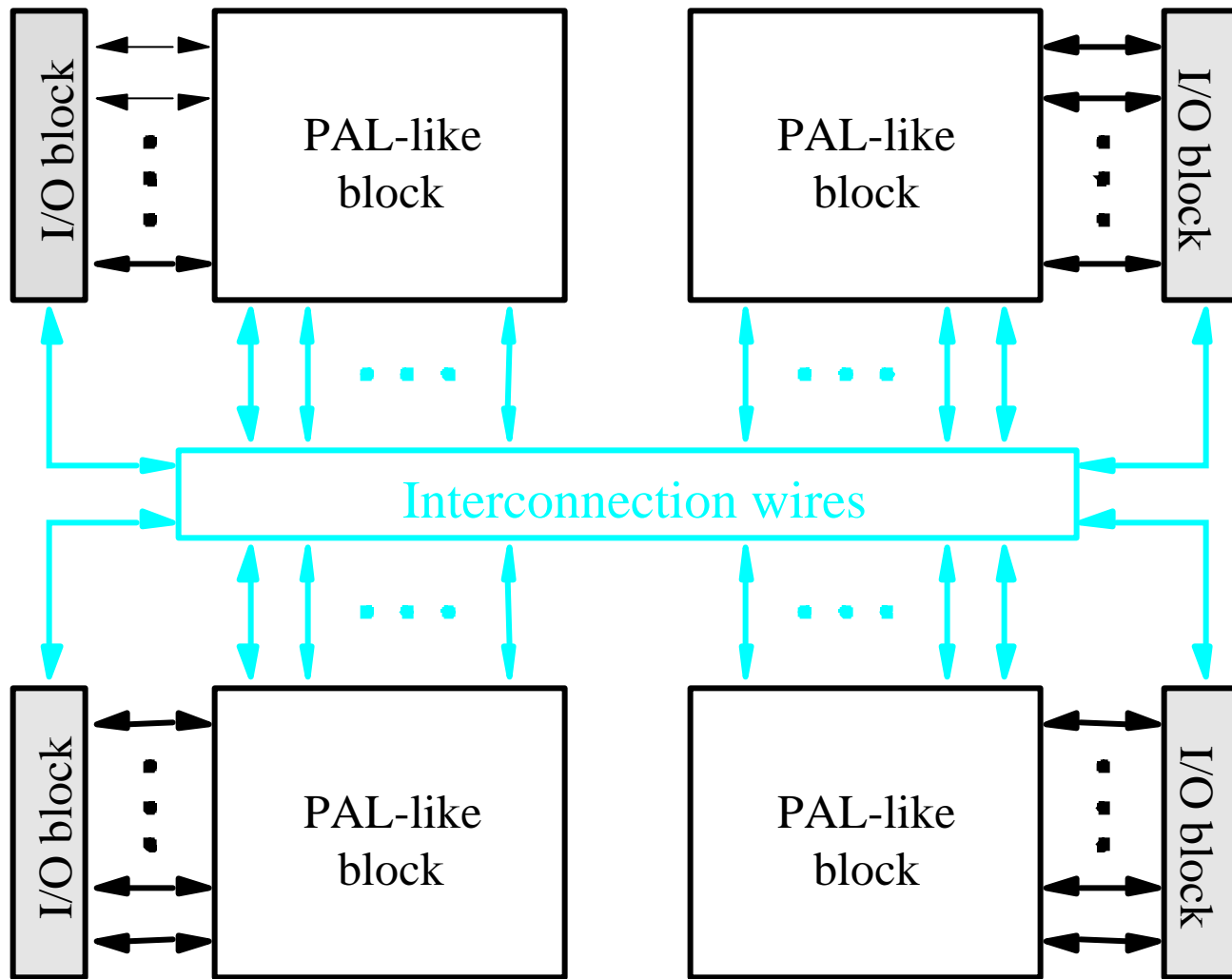
Figure 3.32   Structure of a CPLD
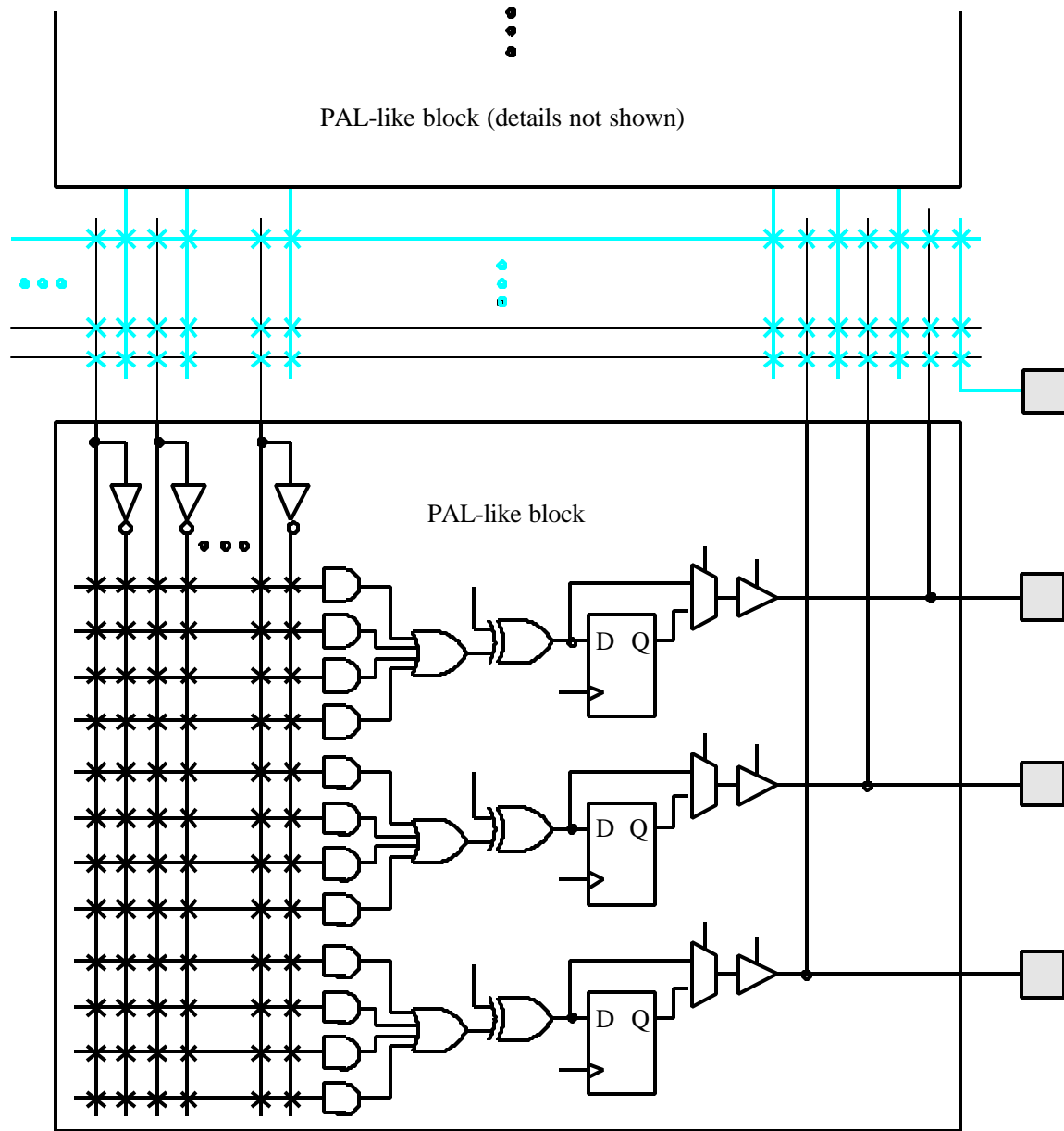
Figure 3.33   A section of a CPLD
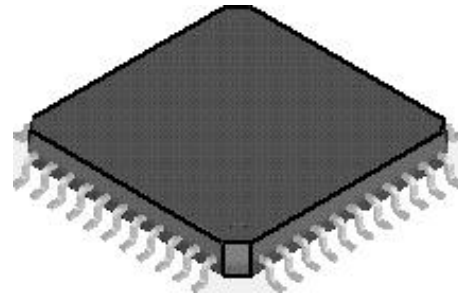
(a) CPLD in a Quad Flat Pack (QFP) package

To computer

Printed
circuit board
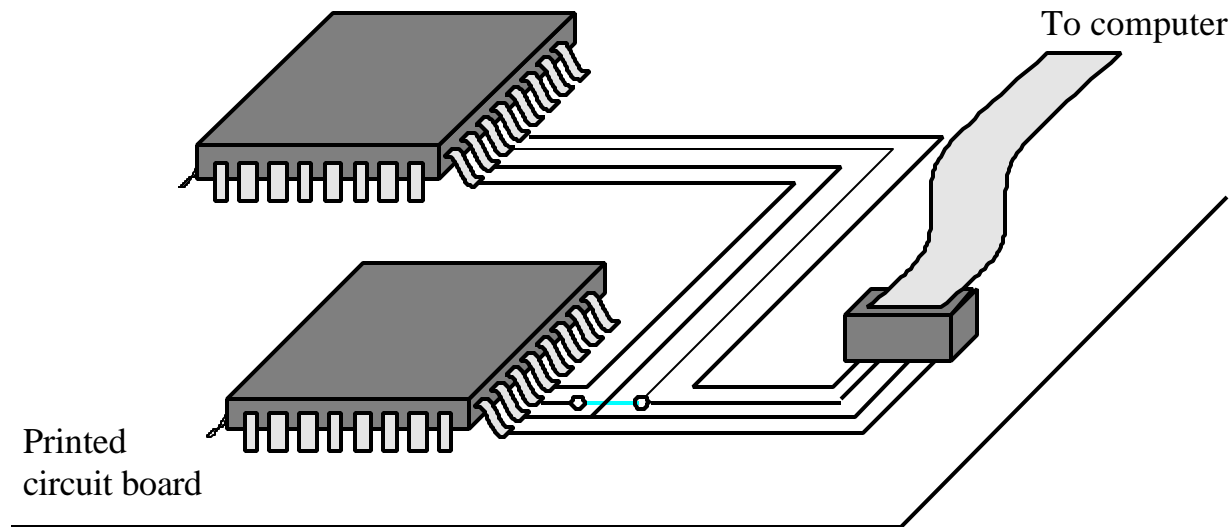
(b) JTAG programming

Figure 3.34   CPLD packaging and programming
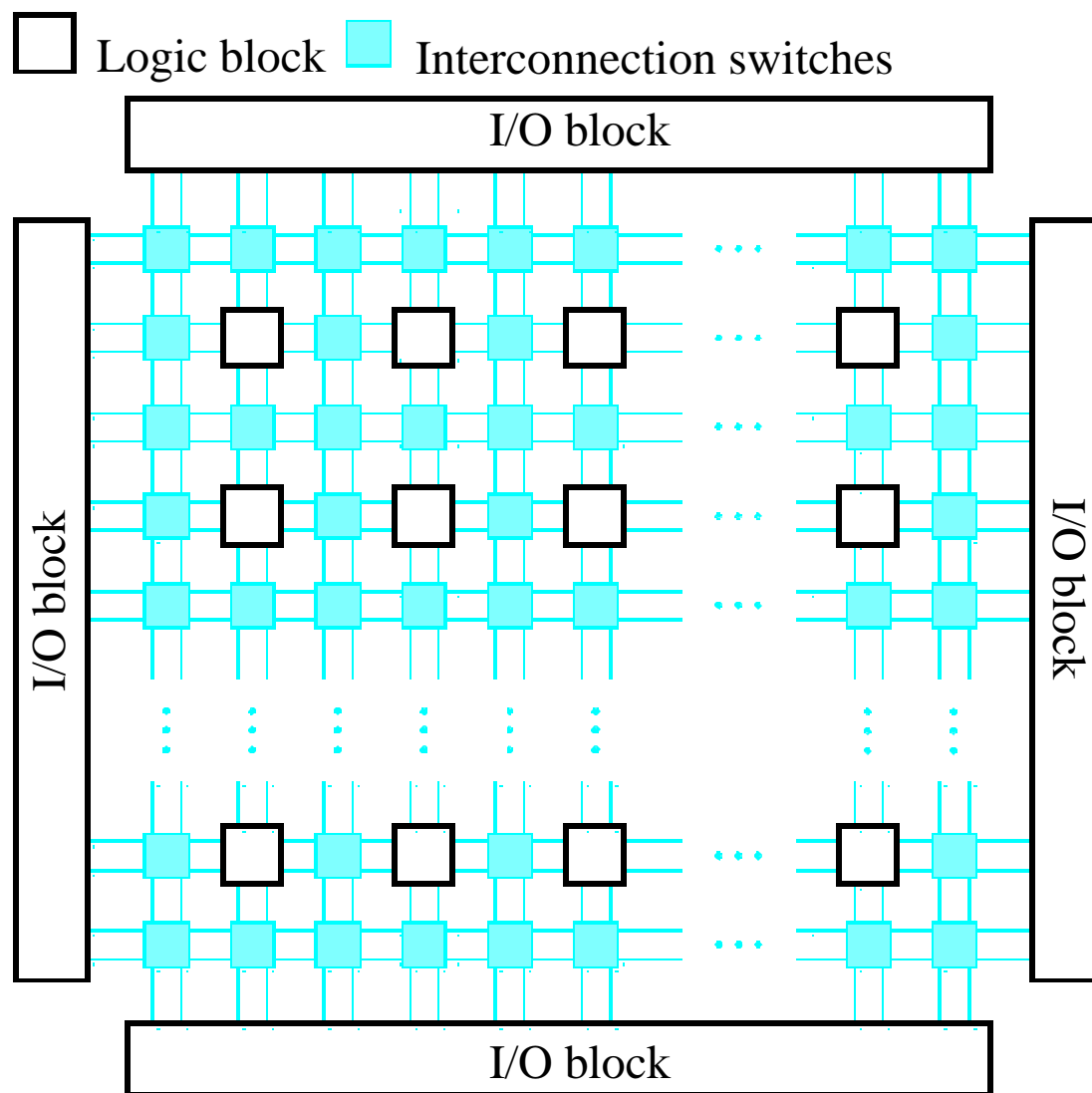
Figure 3.35   Structure of an FPGA
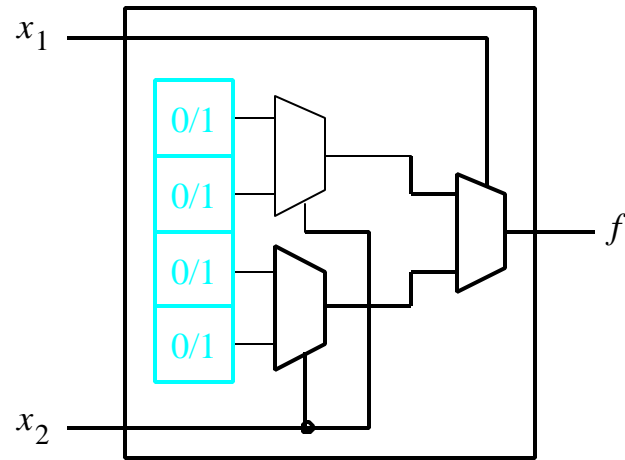
(a) Circuit for a two-input LUT

x_1	x_2	f_1
0	0	1
0	1	0
1	0	0
1	1	1

(b) $f_1 = \bar{x}_1\bar{x}_2 + x_1 x_2$
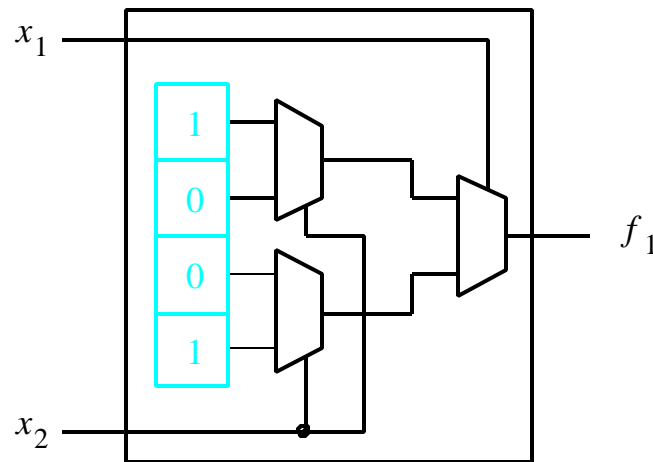
(c) Storage cell contents in the LUT

Figure 3.36   A two-input lookup table
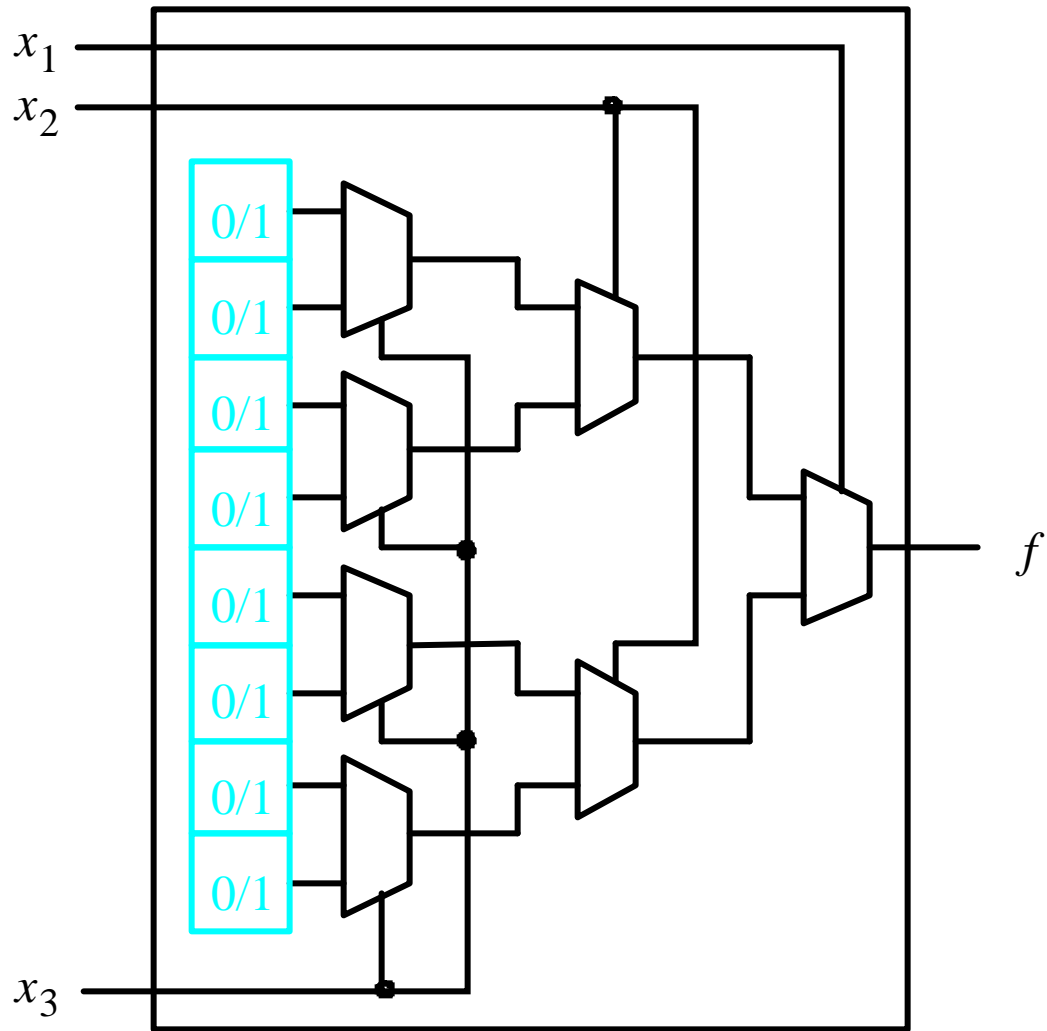
Figure 3.37   A three-input LUT
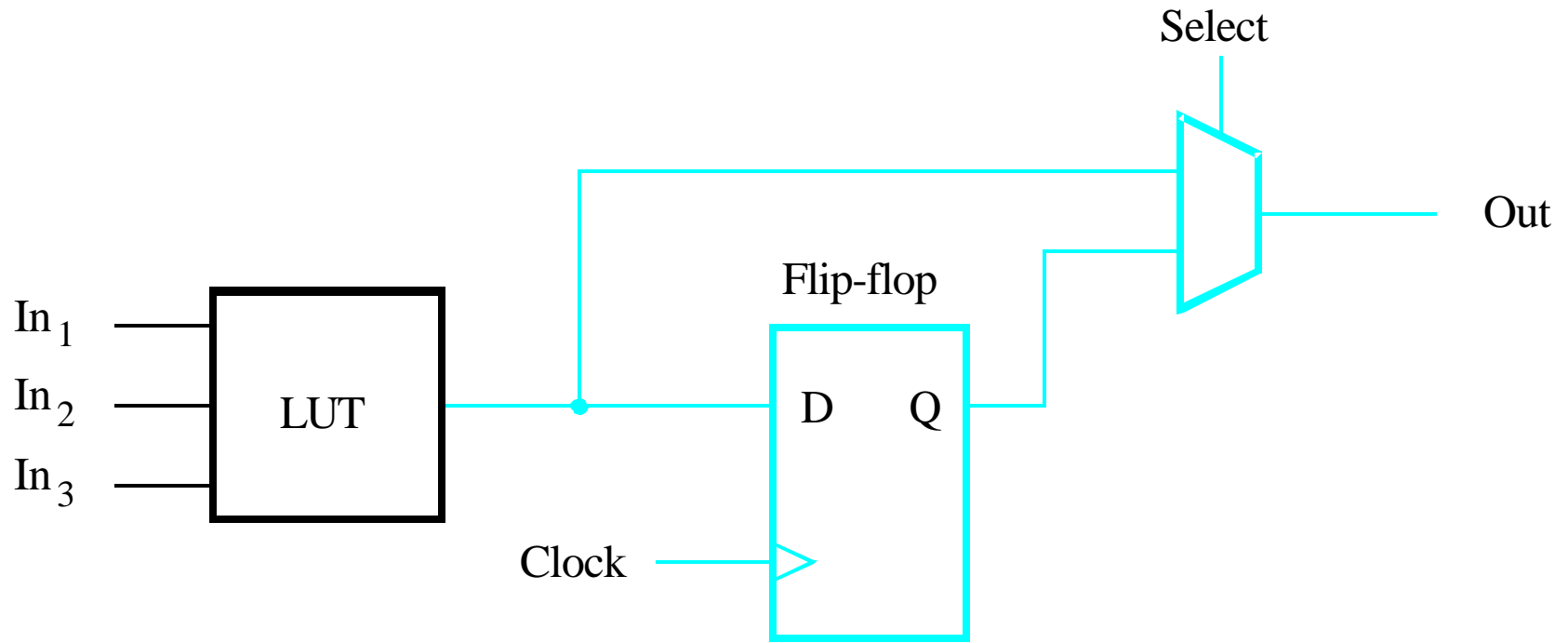
Figure 3.38   Inclusion of a flip-flop with a LUT
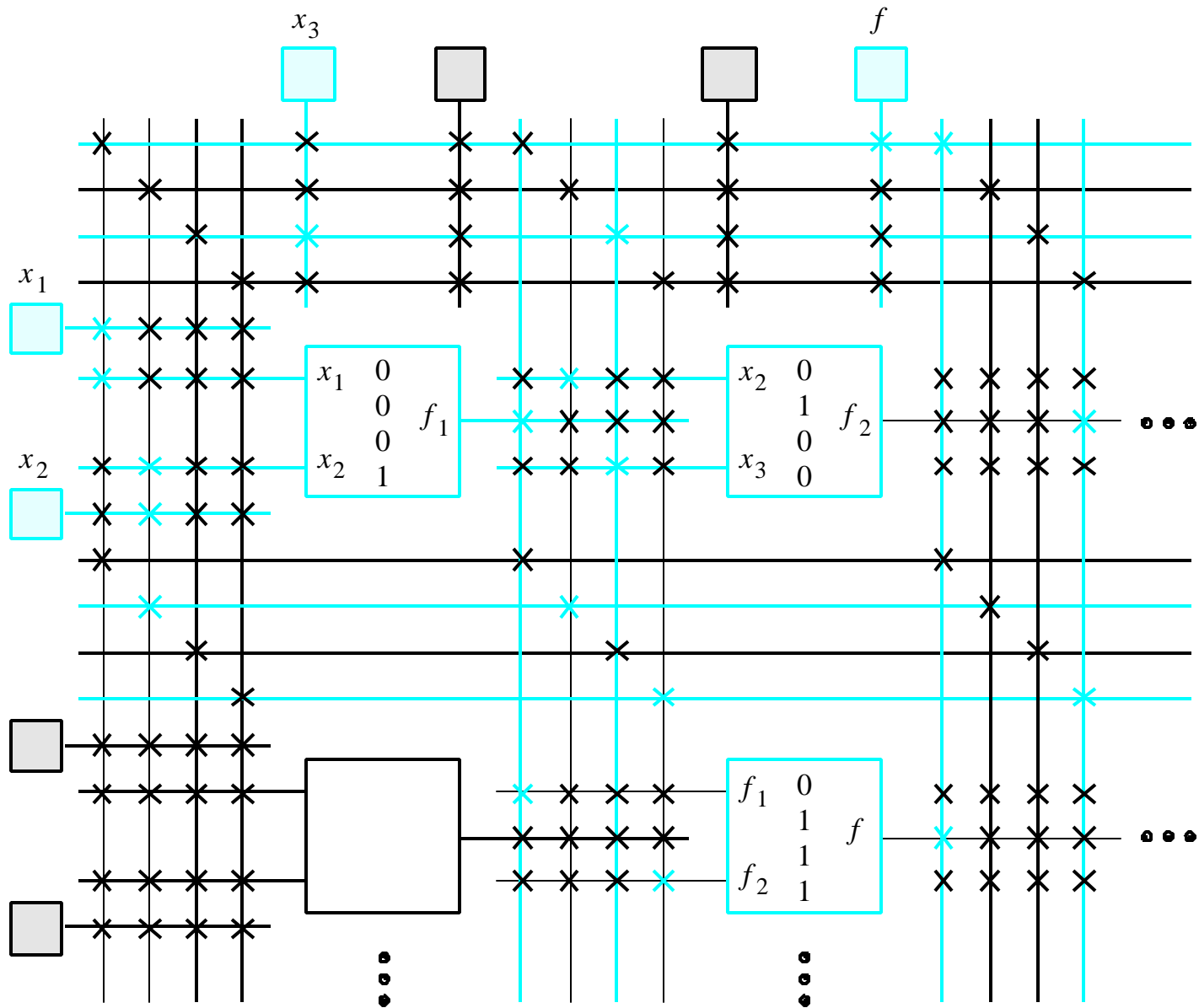
Figure 3.39   A section of a programmed FPGA
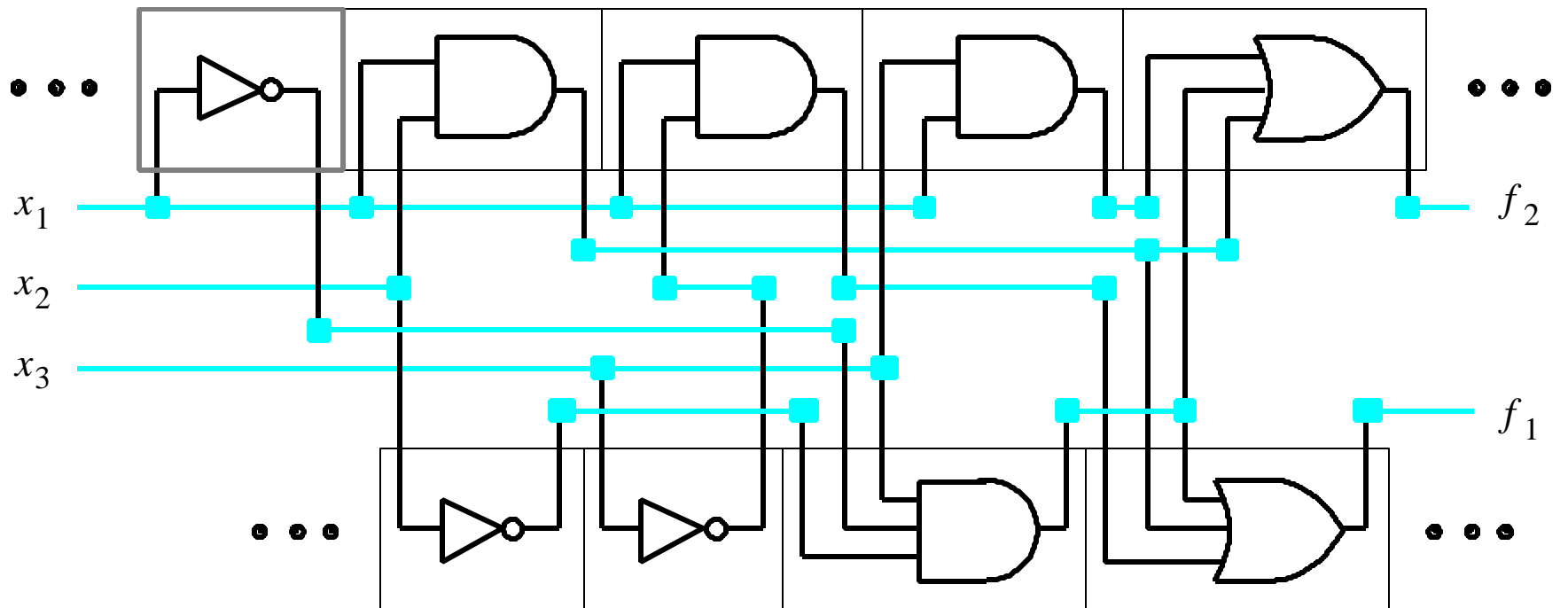
Figure 3.40   A section of two rows in a standard-cell chip
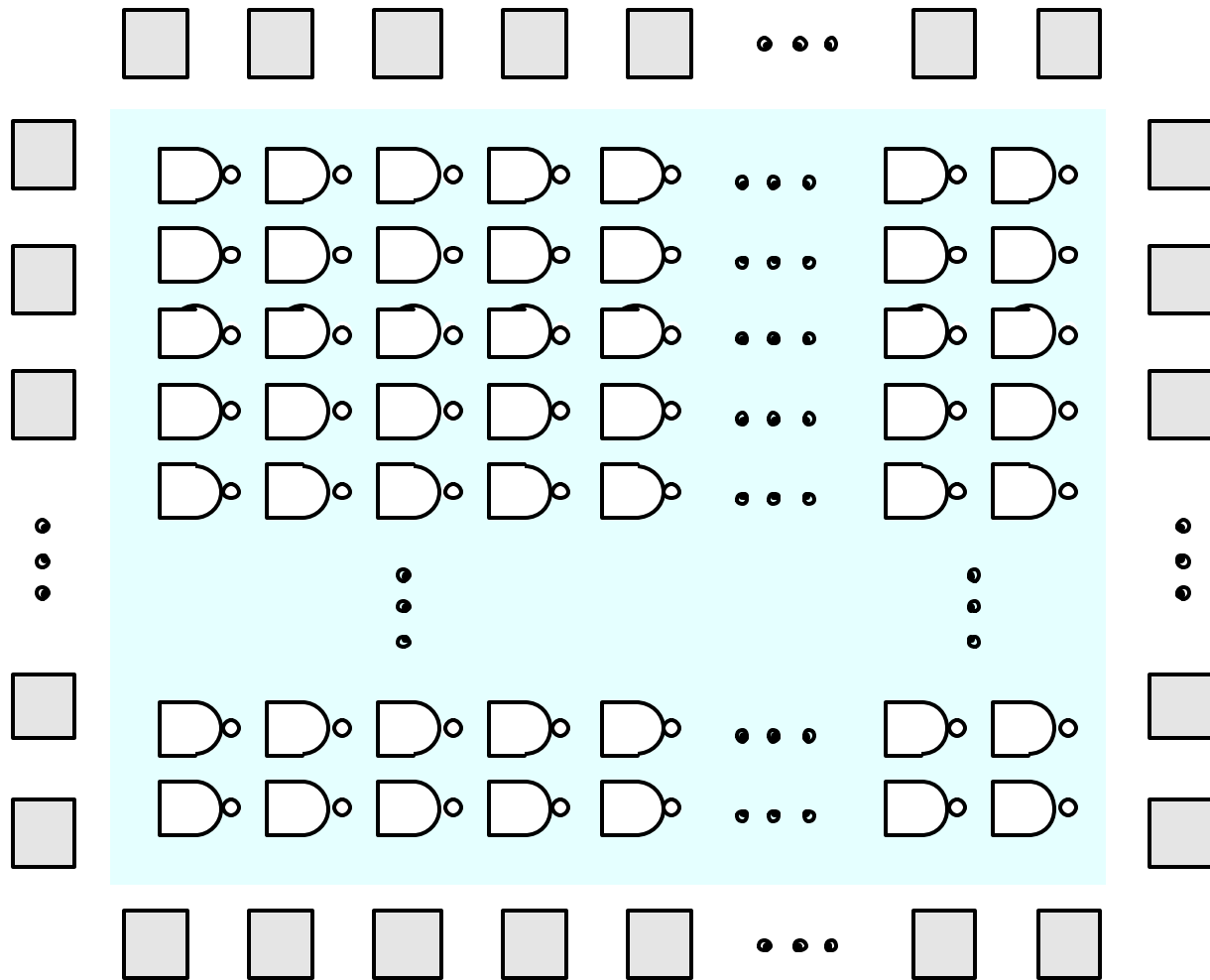
Figure 3.41   A sea-of-gates gate array
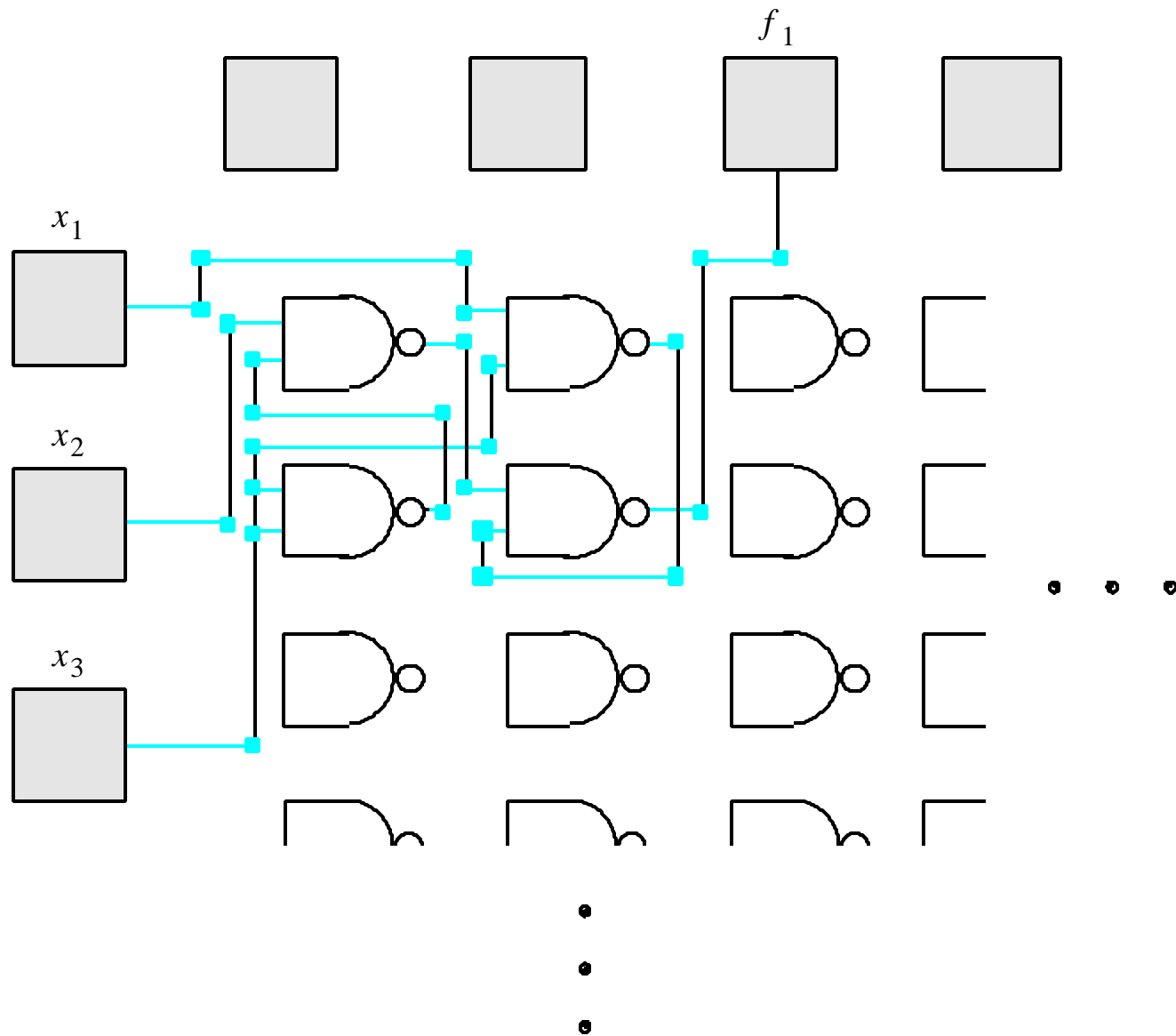
Figure 3.42   An example of a logic function in a gate array

$V_G = 0$ V

SiO $_2$

$V_S = 0$ V

V_D

++++++ — — — ++++++## +++++ — — — ++++++
++++++ ++++++## +++++ ++++++
++++++++++++ ++++++## +++++++## +++++++
+++++++++ Substrate (type p) +++++++++

Source (type n)

Drain (type n)
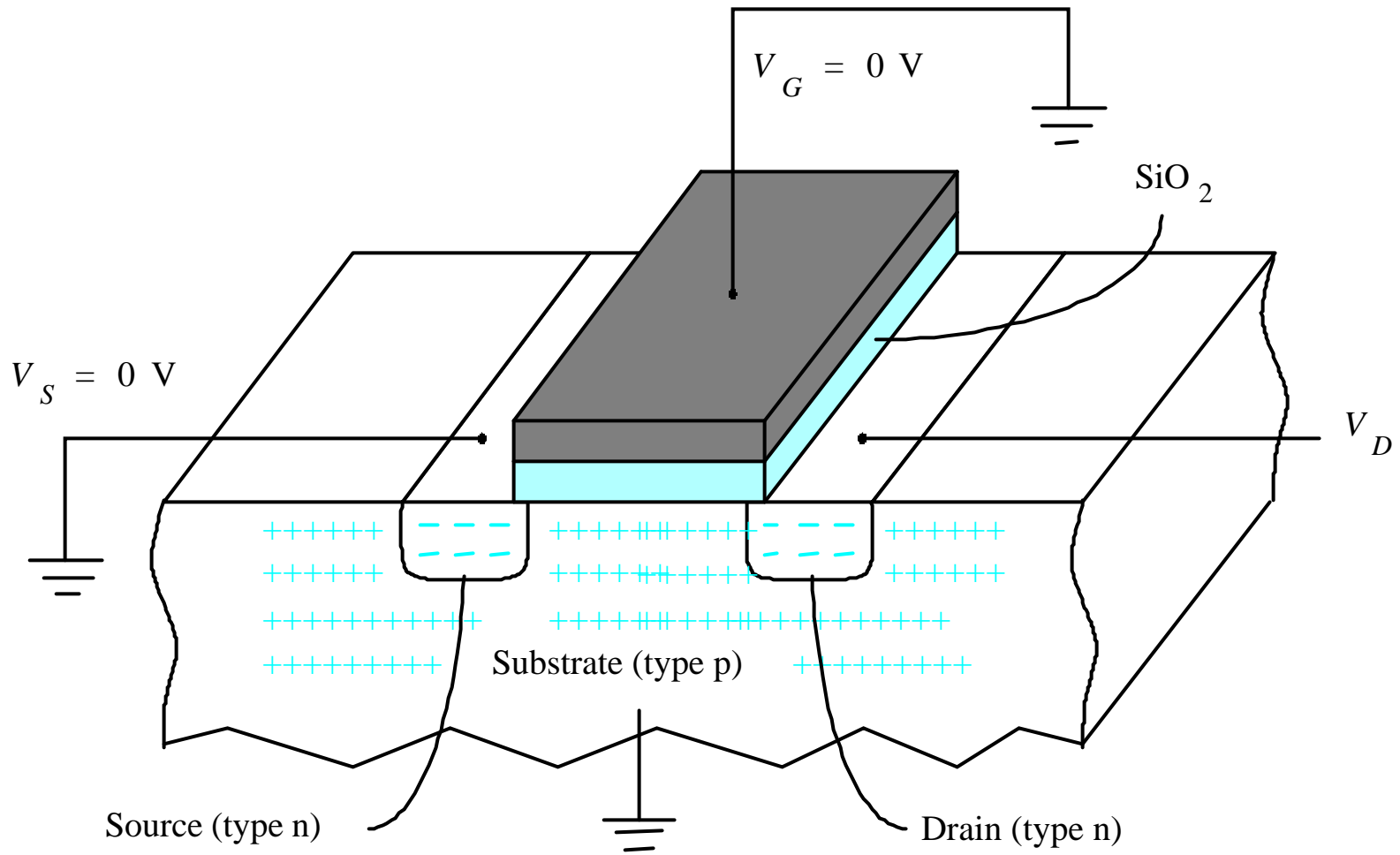
(a) When $V_{GS} = 0$ V, the transistor is off

Figure 3.43 a   NMOS transistor when turned off

V_{DD}

$V_G = 5\ V$

SiO$_2$

$V_S = 0\ V$

$V_D = 0\ V$

Channel (type n)
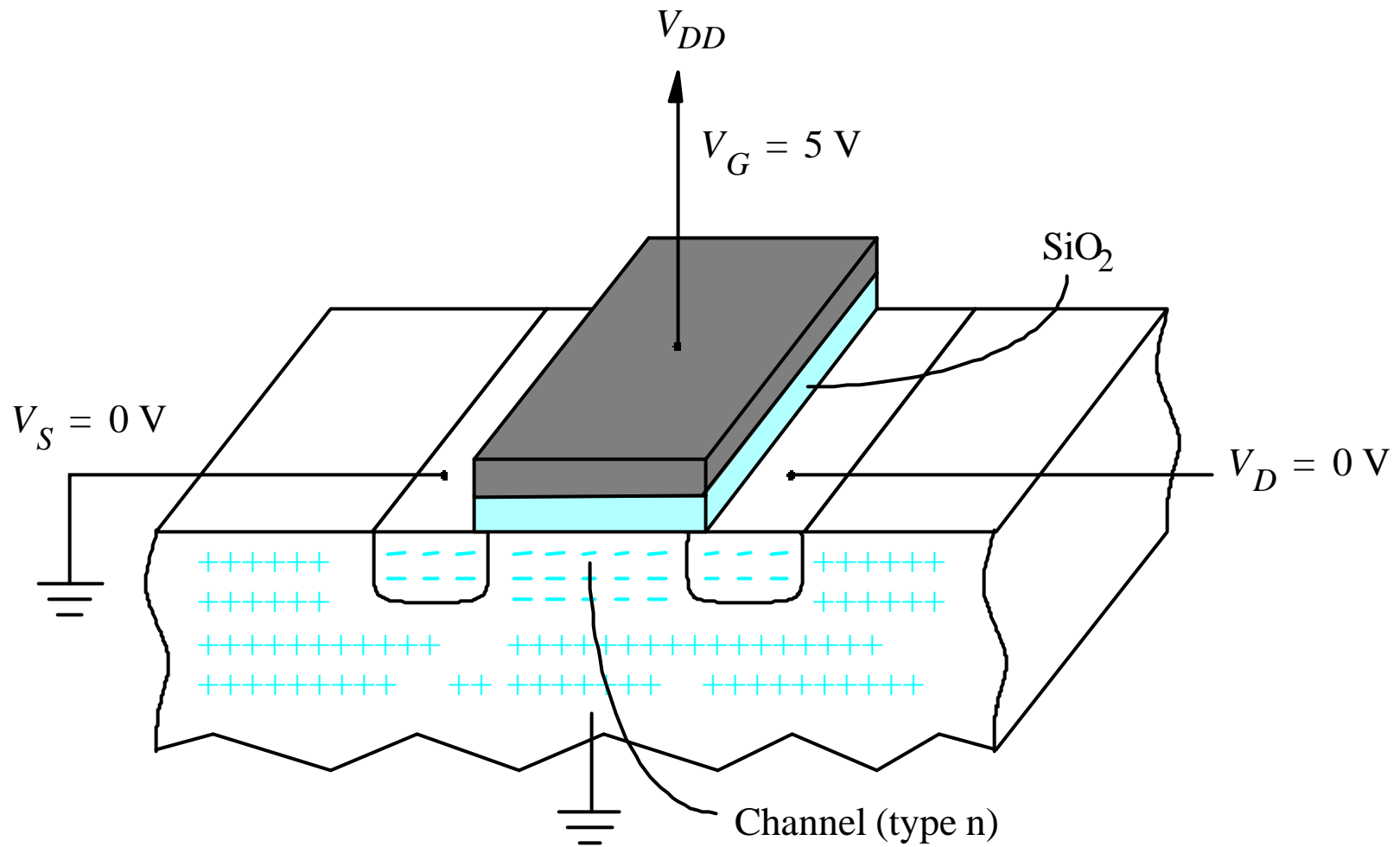
(b) When $V_{GS} = 5\ V$, the transistor is on

Figure 3.43 b   NMOS transistor when turned on
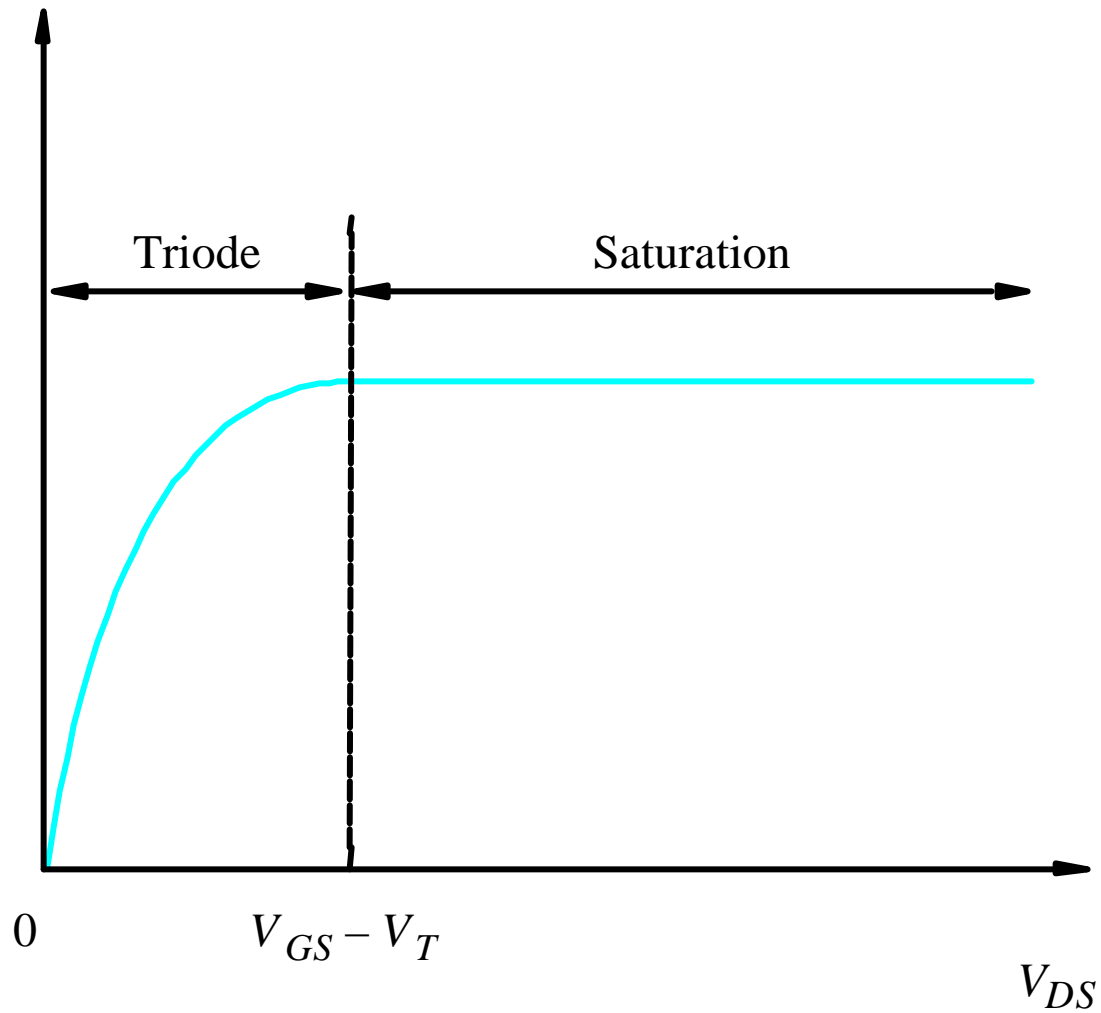
Figure 3.44   Current-voltage relationship in the NMOS transistor

V_{DD}

V_f

V_x

(a) NMOS NOT gate

V_{DD}

R

I_{stat}

$V_f = V_{OL}$

R_{DS}
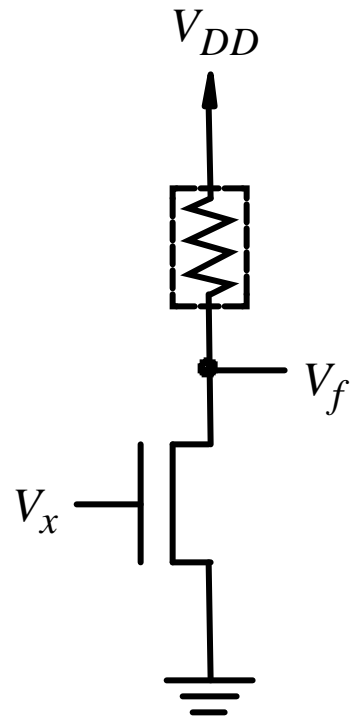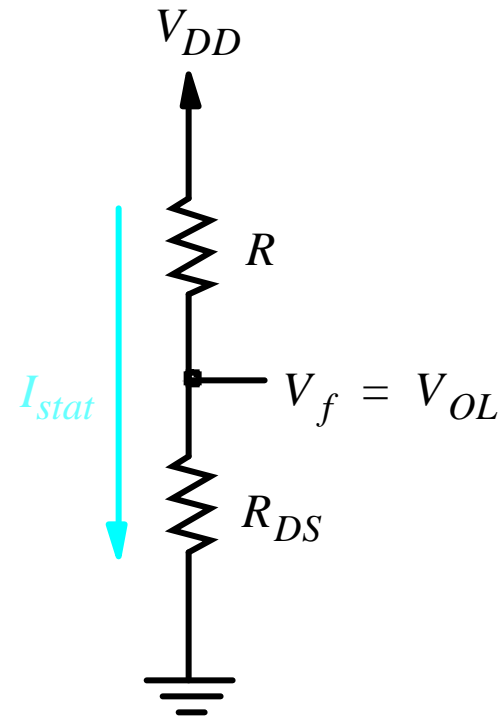
(b) $V_x = 5$ V

Figure 3.45   Voltage levels in the NMOS inverter
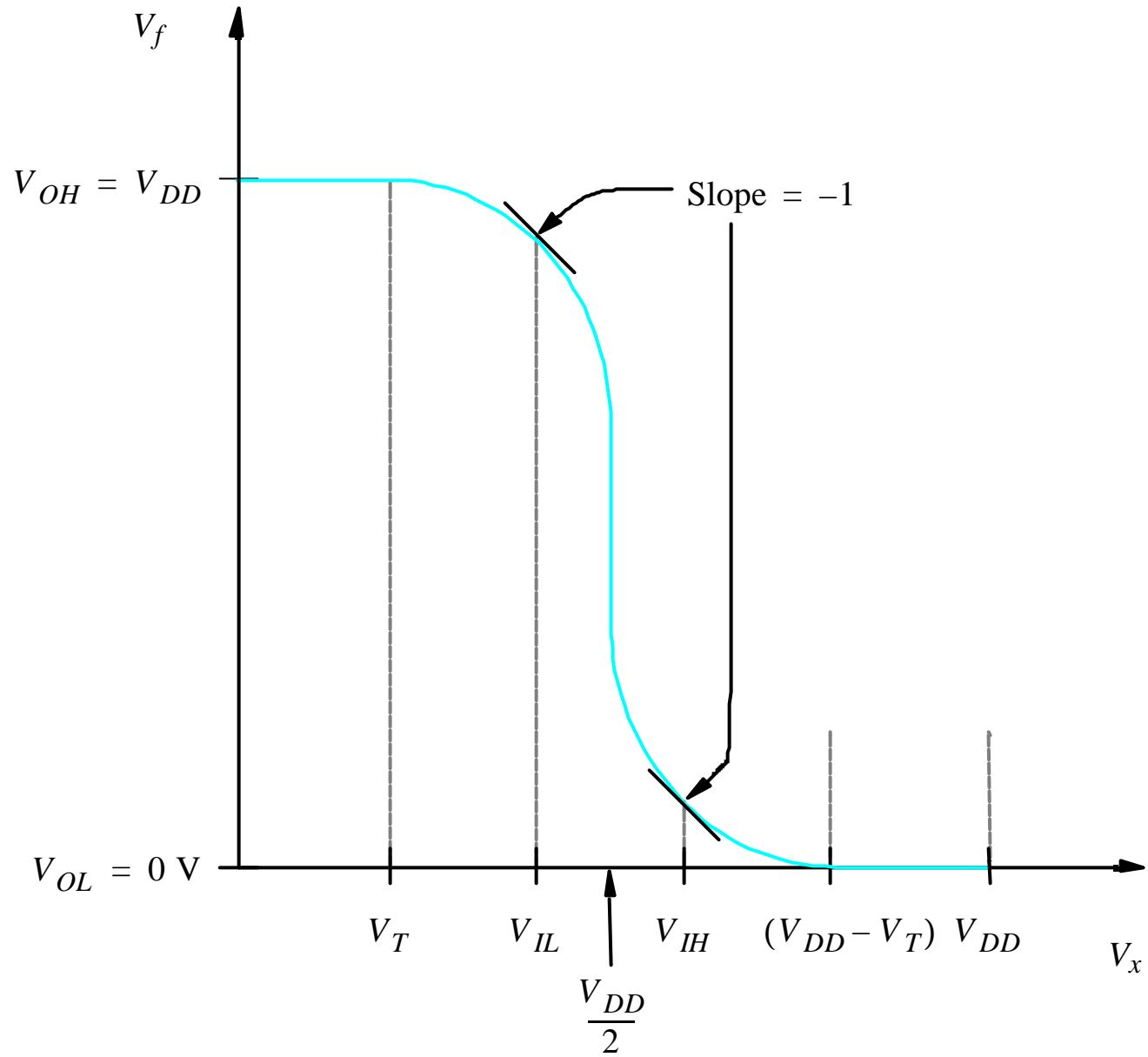
Figure 3.46   Voltage transfer characteristics for the CMOS inverter
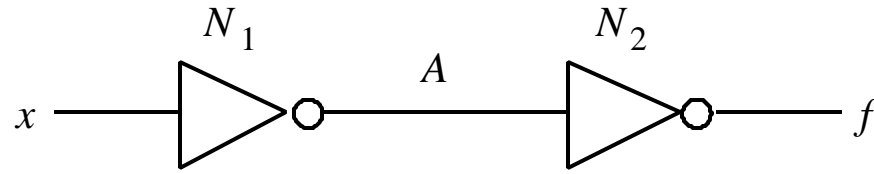
(a) A NOT gate driving another NOT gate
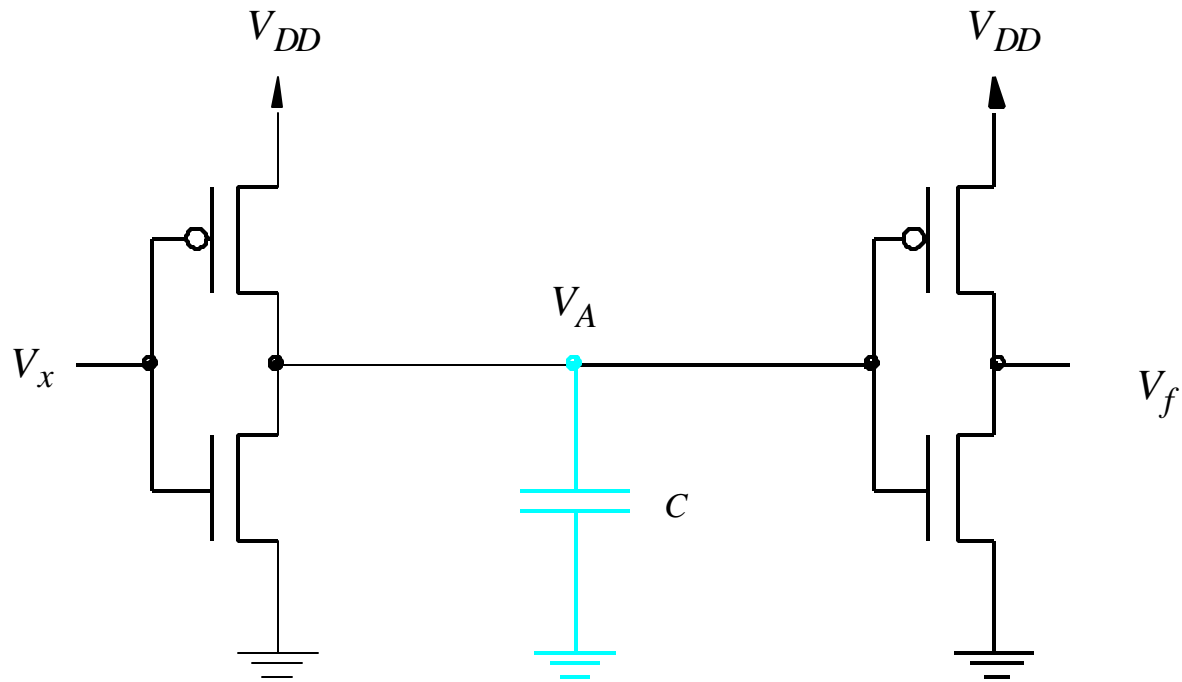
(b) The capacitive load at node A

Figure 3.47   Parasitic capacitance in integrated circuits
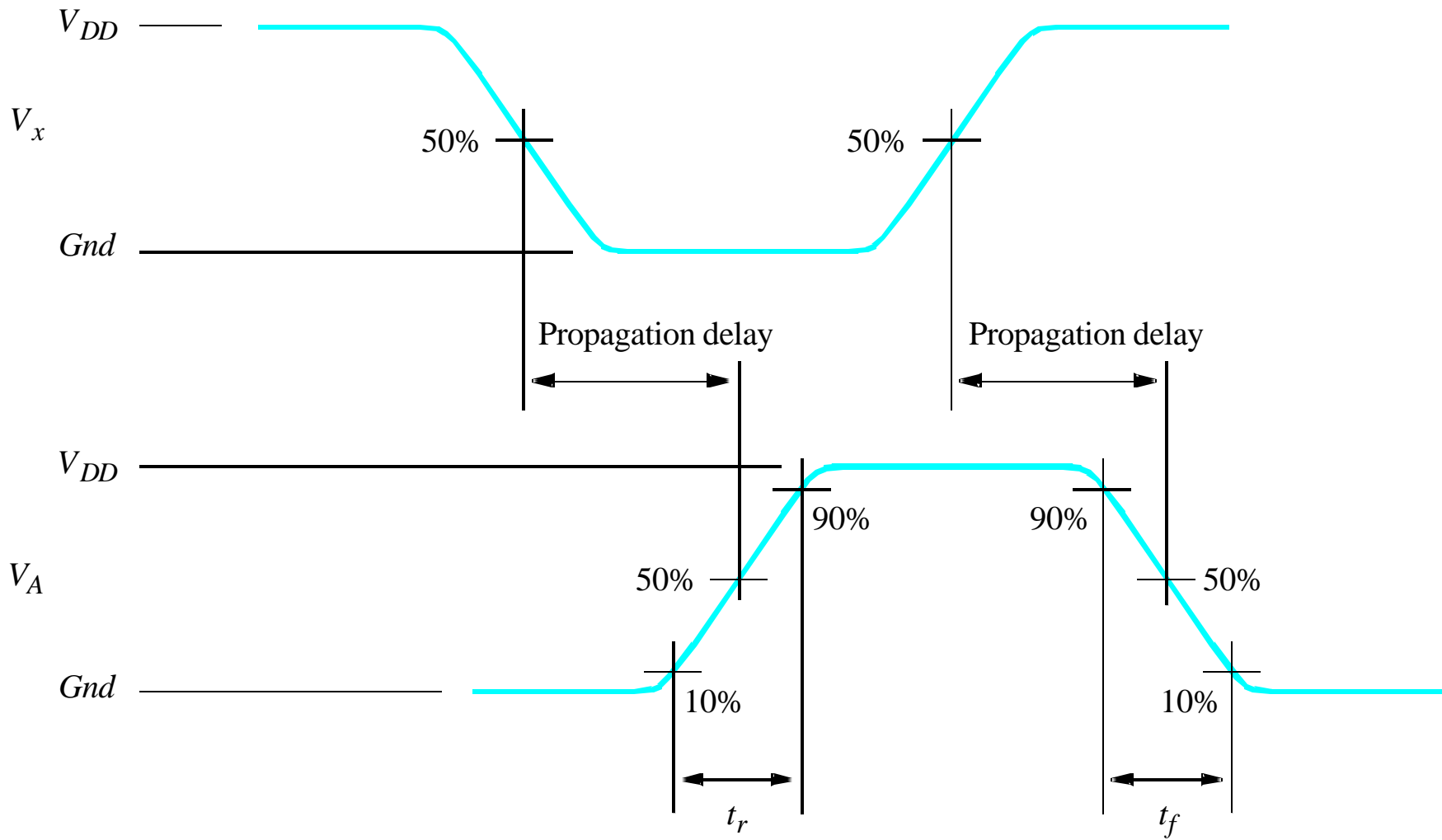
Figure 3.48   Voltage waveforms for logic gates
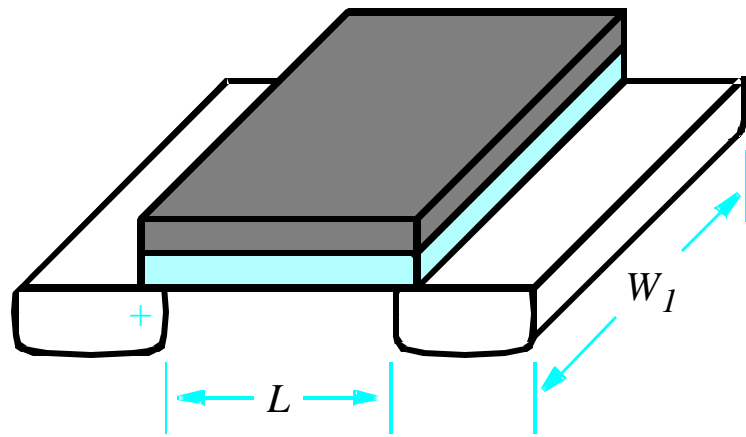
(a) Small transistor
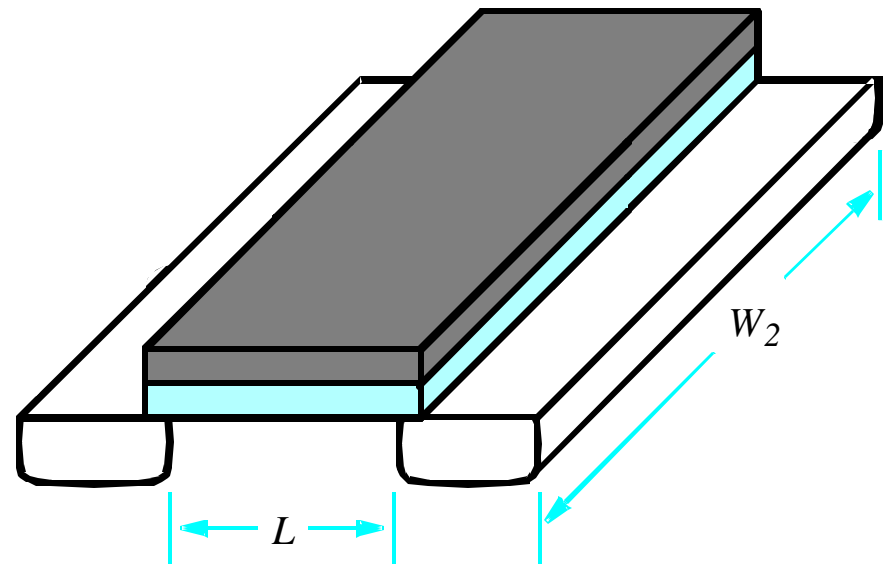
(b) Larger transistor

Figure 3.49 Transistor sizes
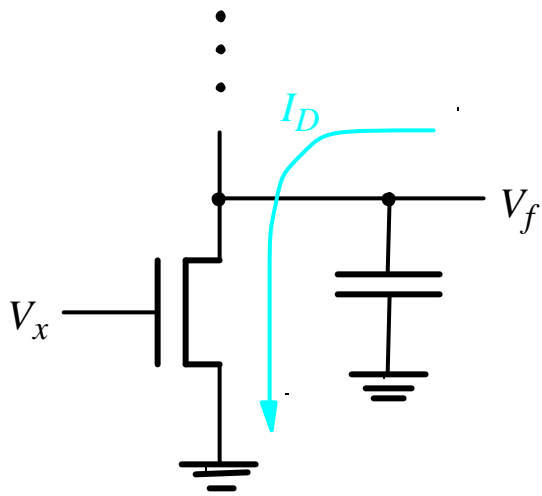
(a) Current flow when input V_x
changes from 0 V to 5 V
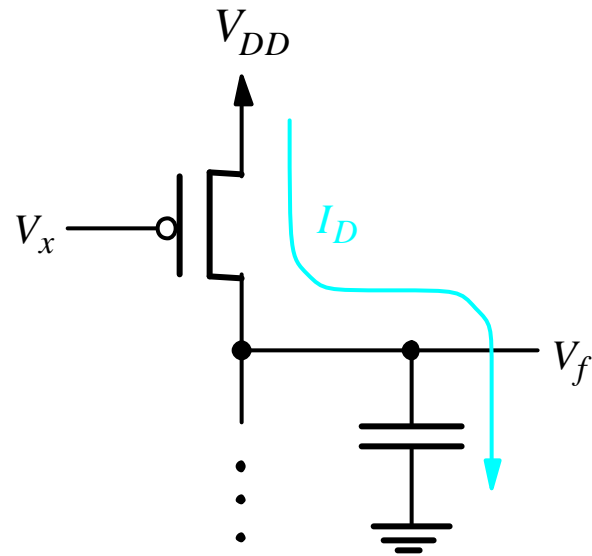
(b) Current flow when input V_x
changes from 5 V to 0 V

Figure 3.50   Dynamic current flow in CMOS circuits
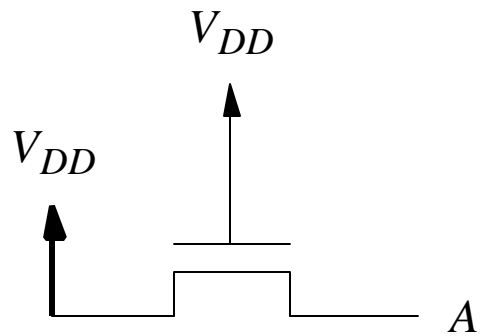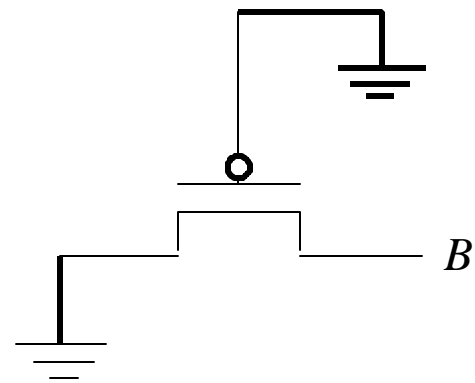
(a) NMOS transistor   (b) PMOS transistor

Figure 3.51   Poor use of NMOS and PMOS transistors
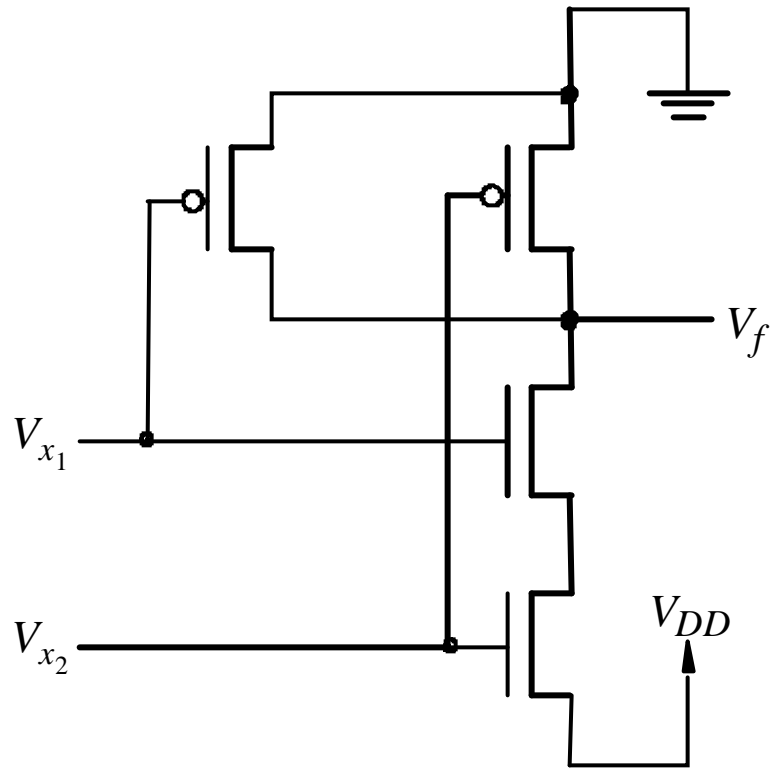
Logic value		Voltage	Logic value
x_1	x_2	V_f	f
0	0	1.5 V	0
0	1	1.5 V	0
1	0	1.5 V	0
1	1	3.5 V	1

(a) An AND gate circuit

(b) Truth table and voltage levels

Figure 3.52   Poor implementation of a CMOS AND gate
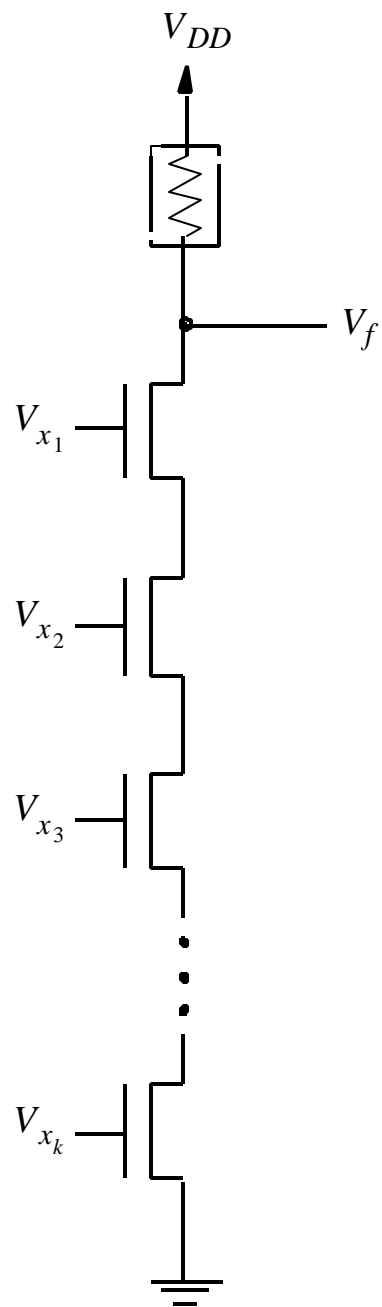
Figure 3.53   High fan-in NMOS NAND gate
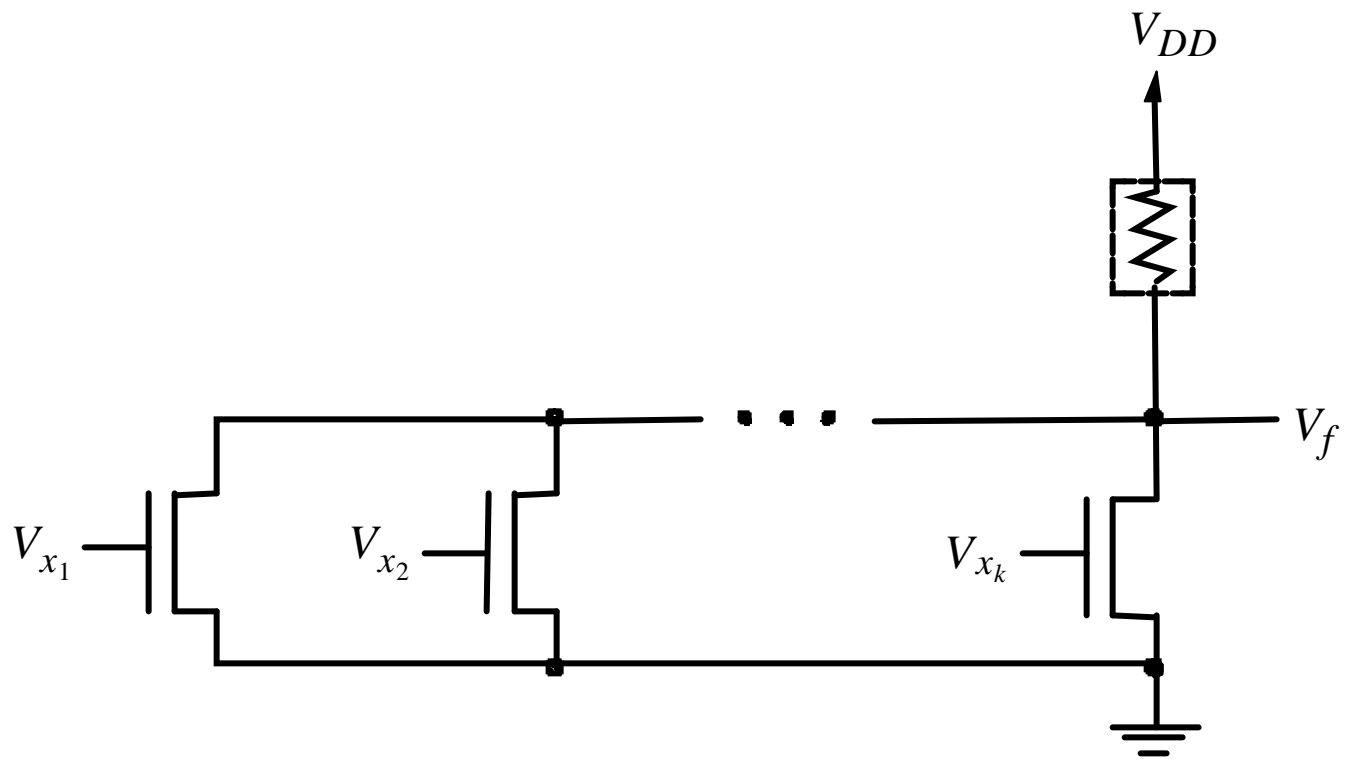
Figure 3.54   High fan-in NMOS NOR gate
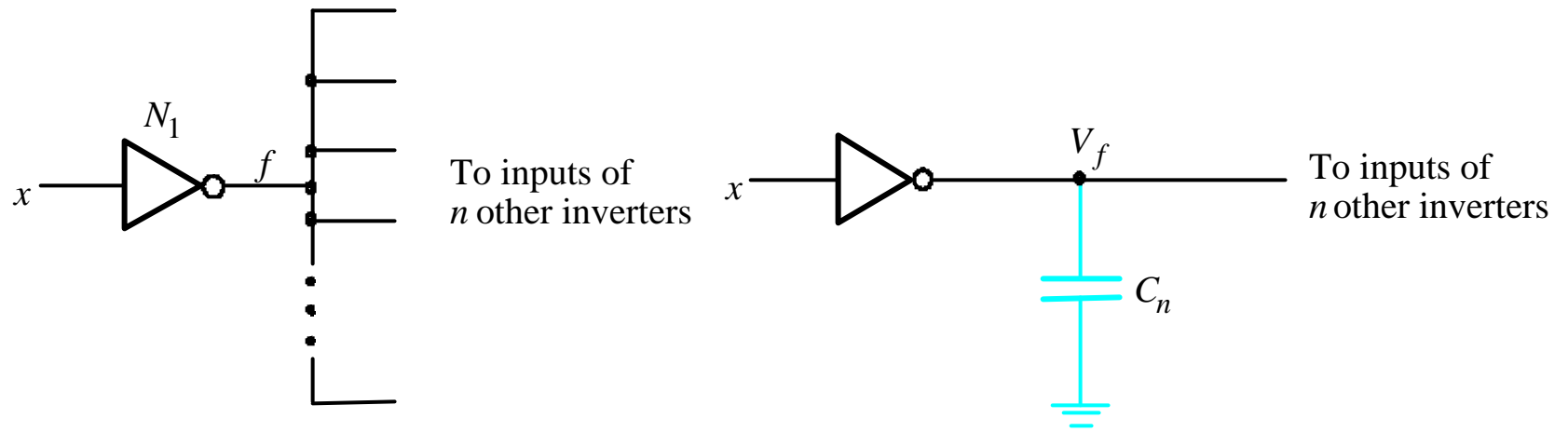
(a) Inverter that drives *n* other inverters

(b) Equivalent circuit for timing purposes
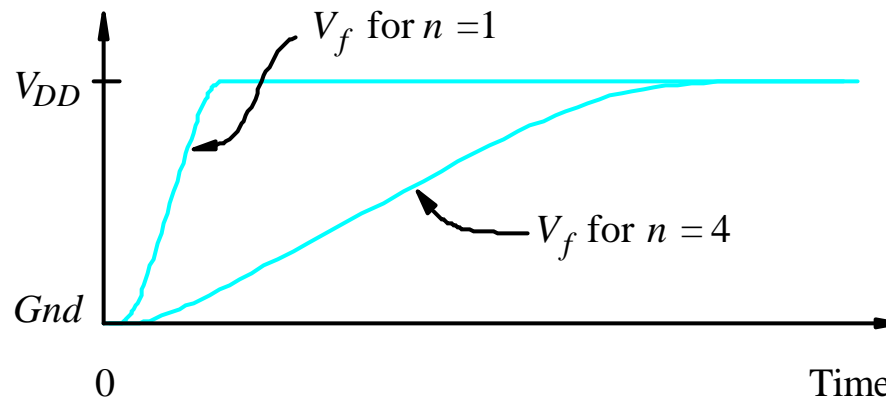
(c) Propagation times for different values of *n*

Figure 3.55   The effect of fan-out on propagation delay
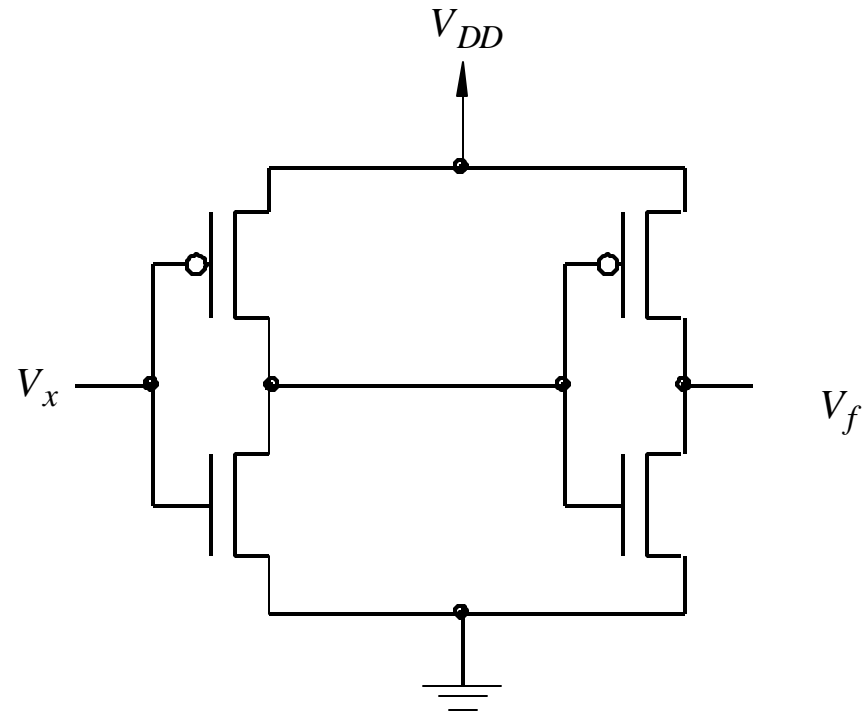
(a) Implementation of a buffer

x ———▷——— f
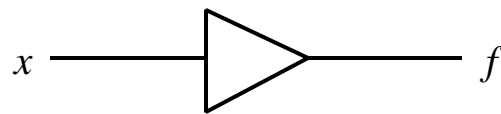
(b) Graphical symbol

Figure 3.56   A noninverting buffer
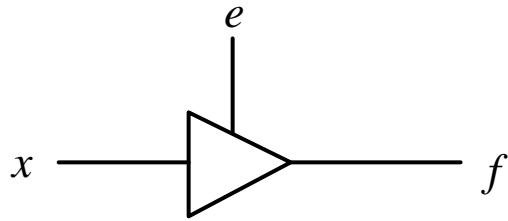
(a) A tri-state buffer
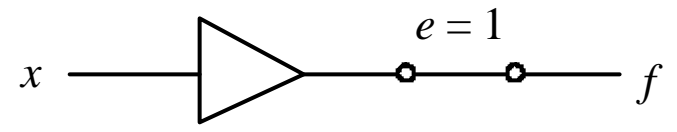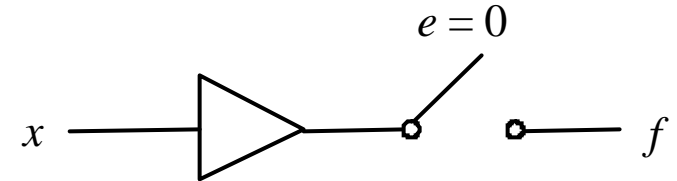
(b) Equivalent circuit

e	x	f
0	0	Z
0	1	Z
1	0	0
1	1	1

(c) Truth table
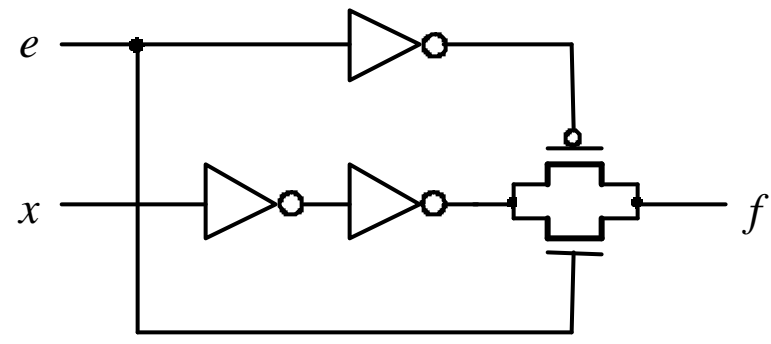
(d) Implementation

Figure 3.57   Tri-state buffer
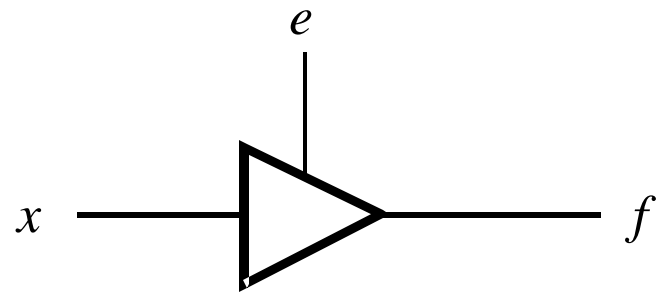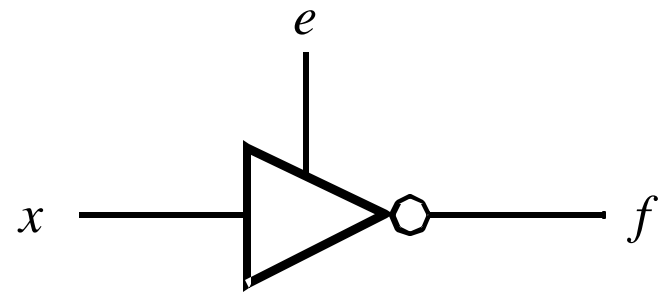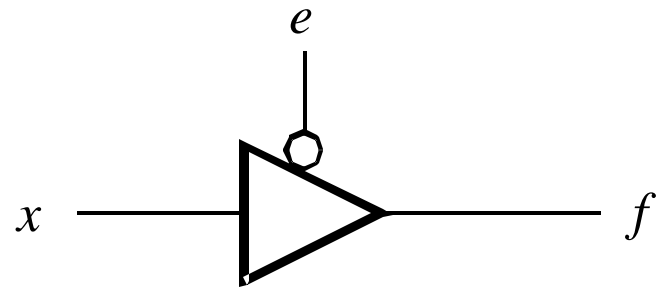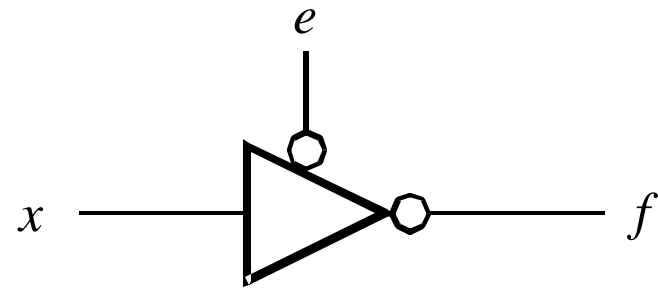
Figure 3.58   Four types of tri-state buffers
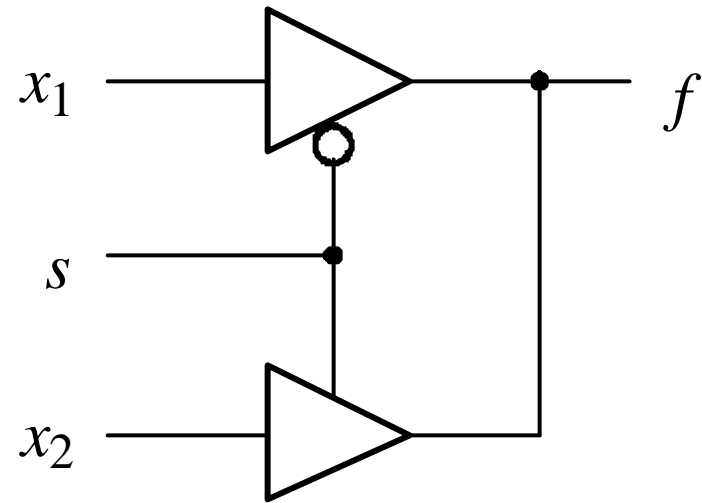
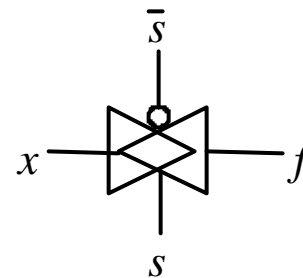Figure 3.59   An application of tri-state buffers
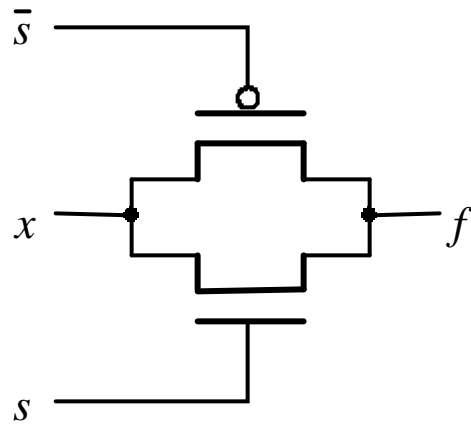
(a) Circuit

s	f
0	Z
1	x

(b) Truth table

$s = 0$

$x \quad \quad f = Z$

$s = 1$

$x \quad \quad f = x$
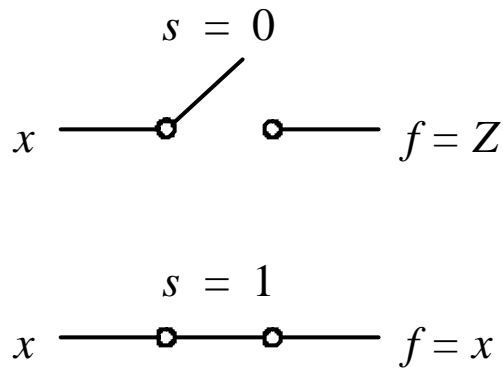
(c) Equivalent circuit

(d) Graphical symbol

Figure 3.60   A transmission gate

x_1	x_2	$f = x_1 \oplus x_2$
0	0	0
0	1	1
1	0	1
1	1	0

(a) Truth table

$f = x_1 \oplus x_2$

(b) Graphical symbol

$f = x_1 \oplus x_2$
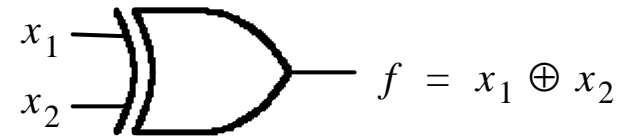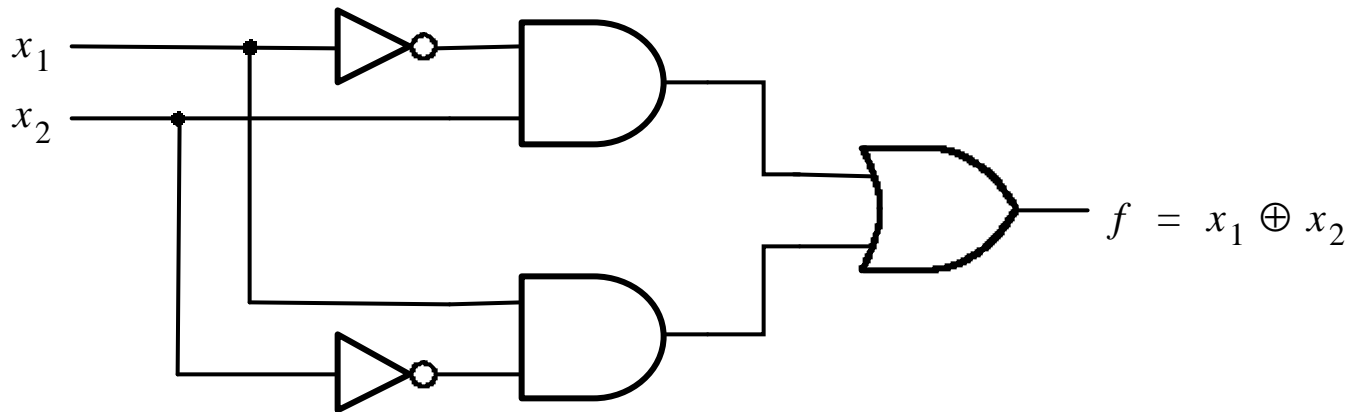
(c) Sum-of-products implementation

Figure 3.61 a   Exclusive-OR gate
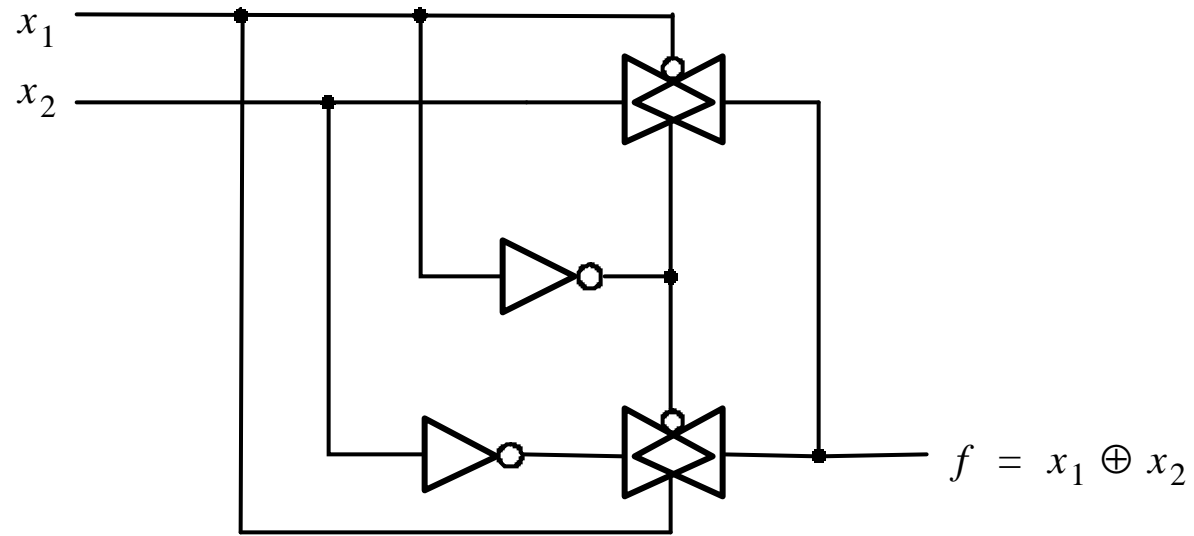
(d) CMOS implementation

Figure 3.61 b   CMOS Exclusive-OR gate
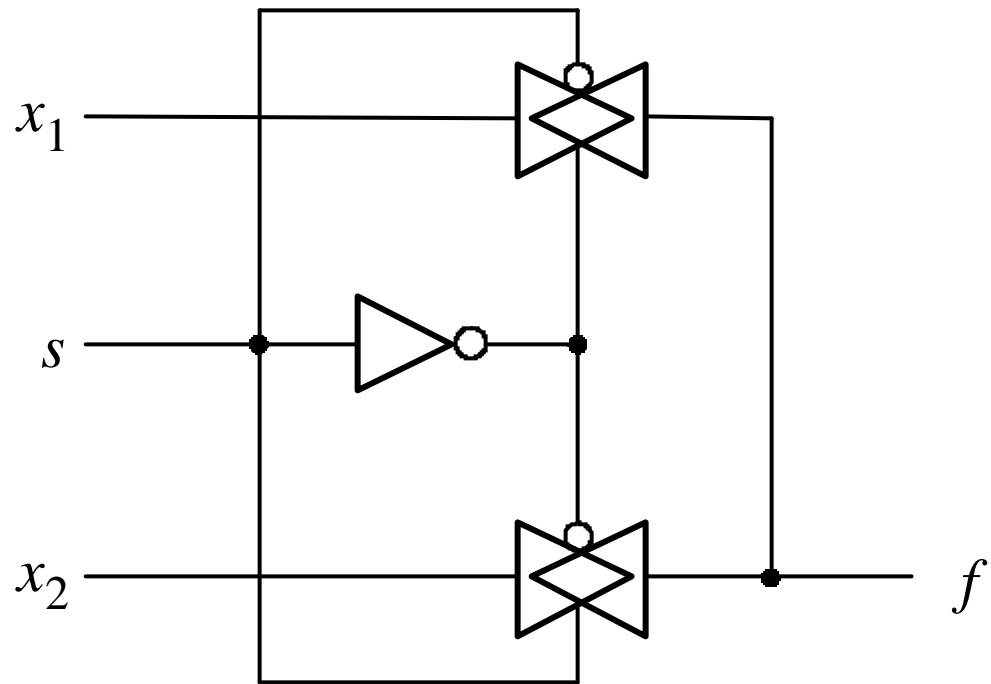
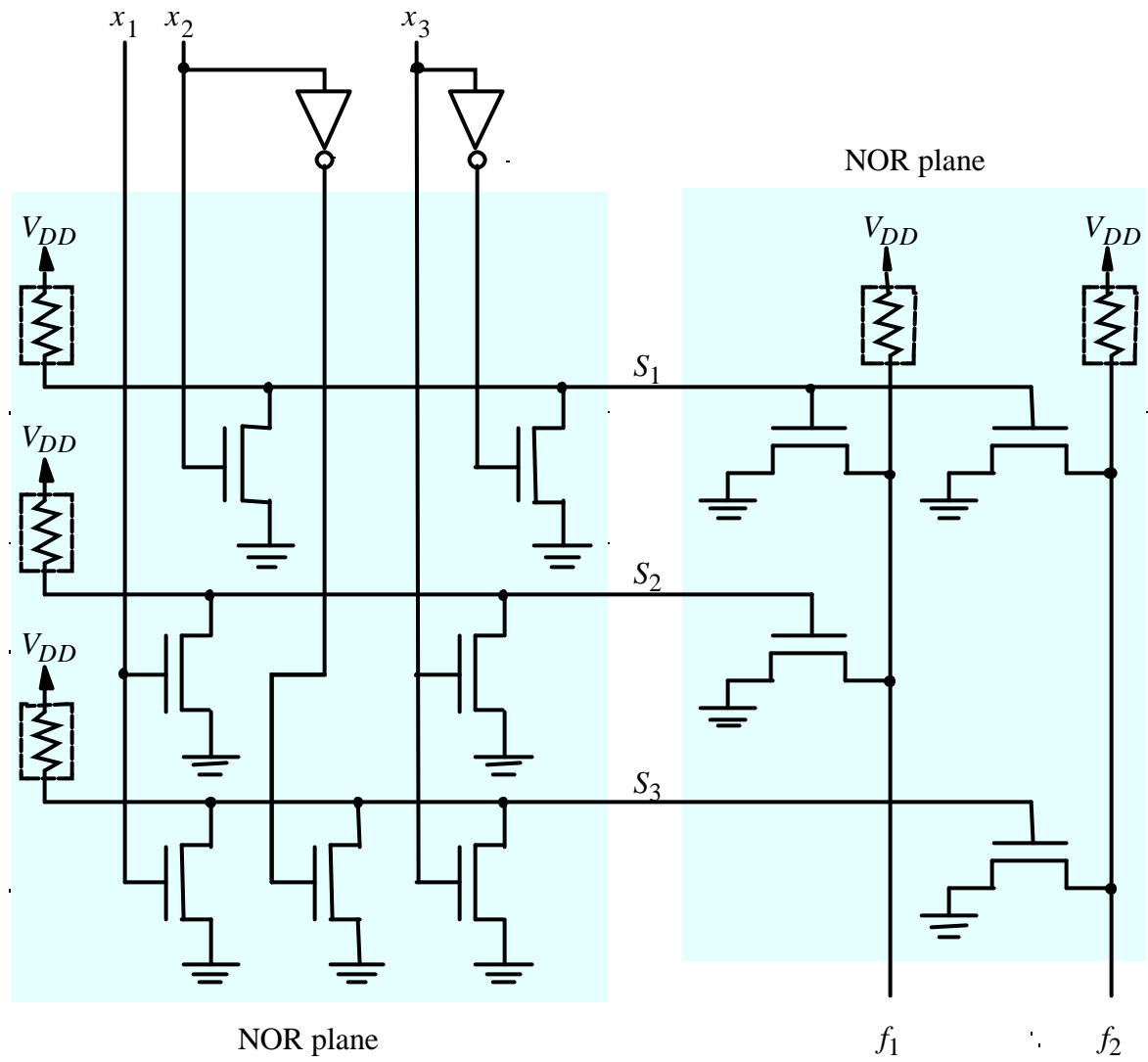Figure 3.62   A 2-to-1 multiplexer built using transmission gates

Figure 3.63   An example of a NOR-NOR PLA

Please see "portrait orientation" PowerPoint file for Chapter 3

Figure 3.64 A programmable NOR plane
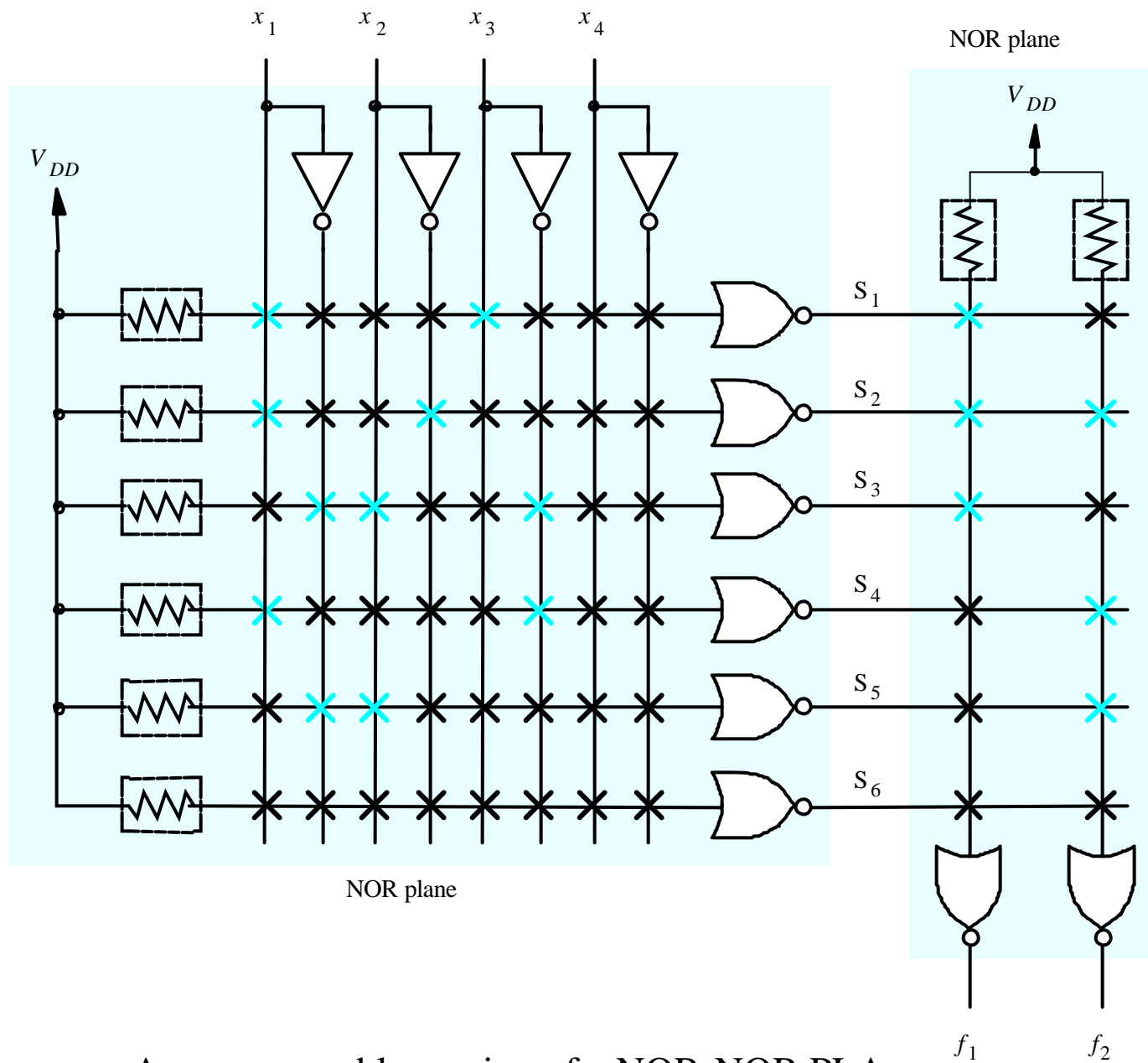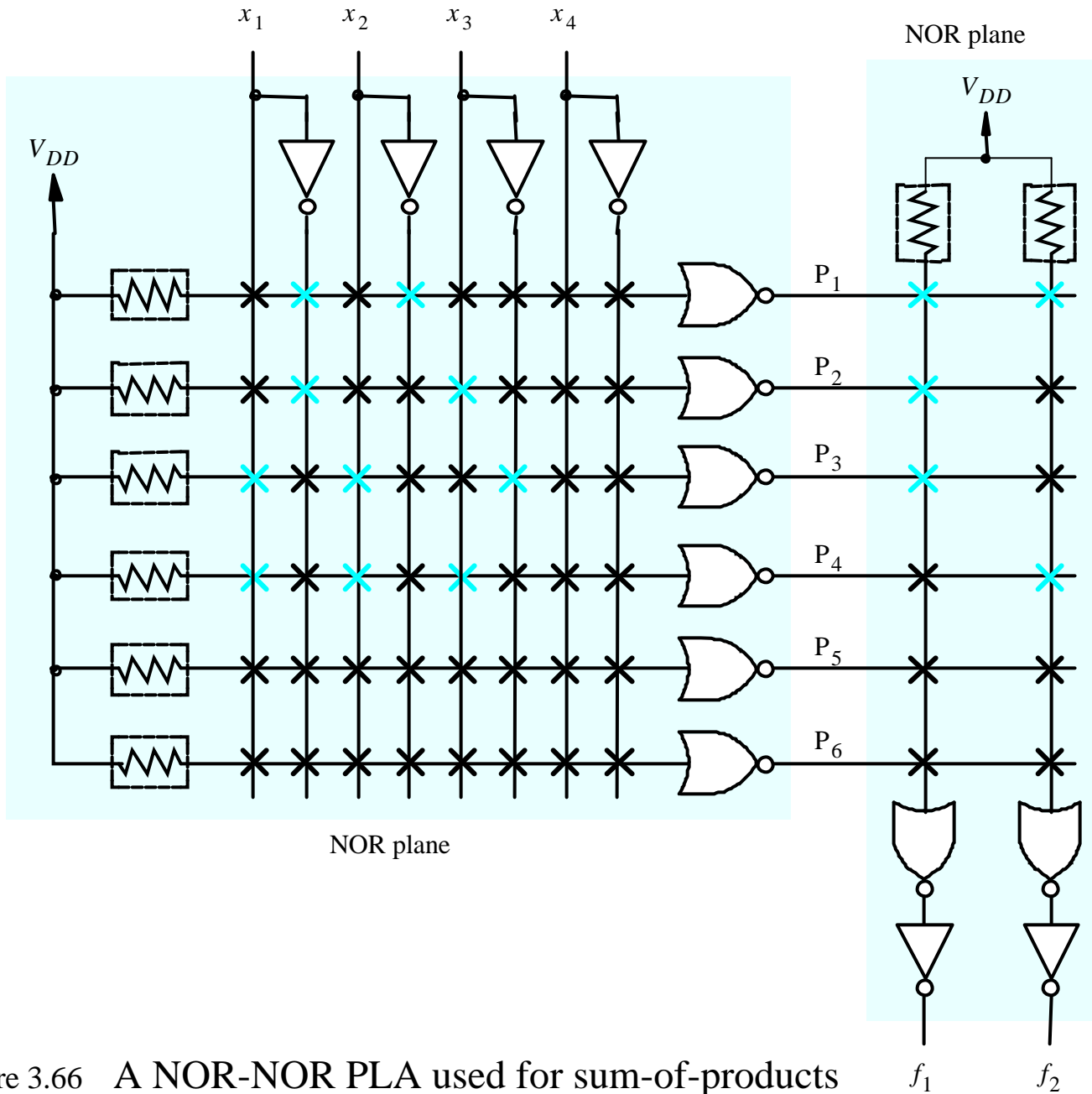
Figure 3.65   A programmable version of a NOR-NOR PLA
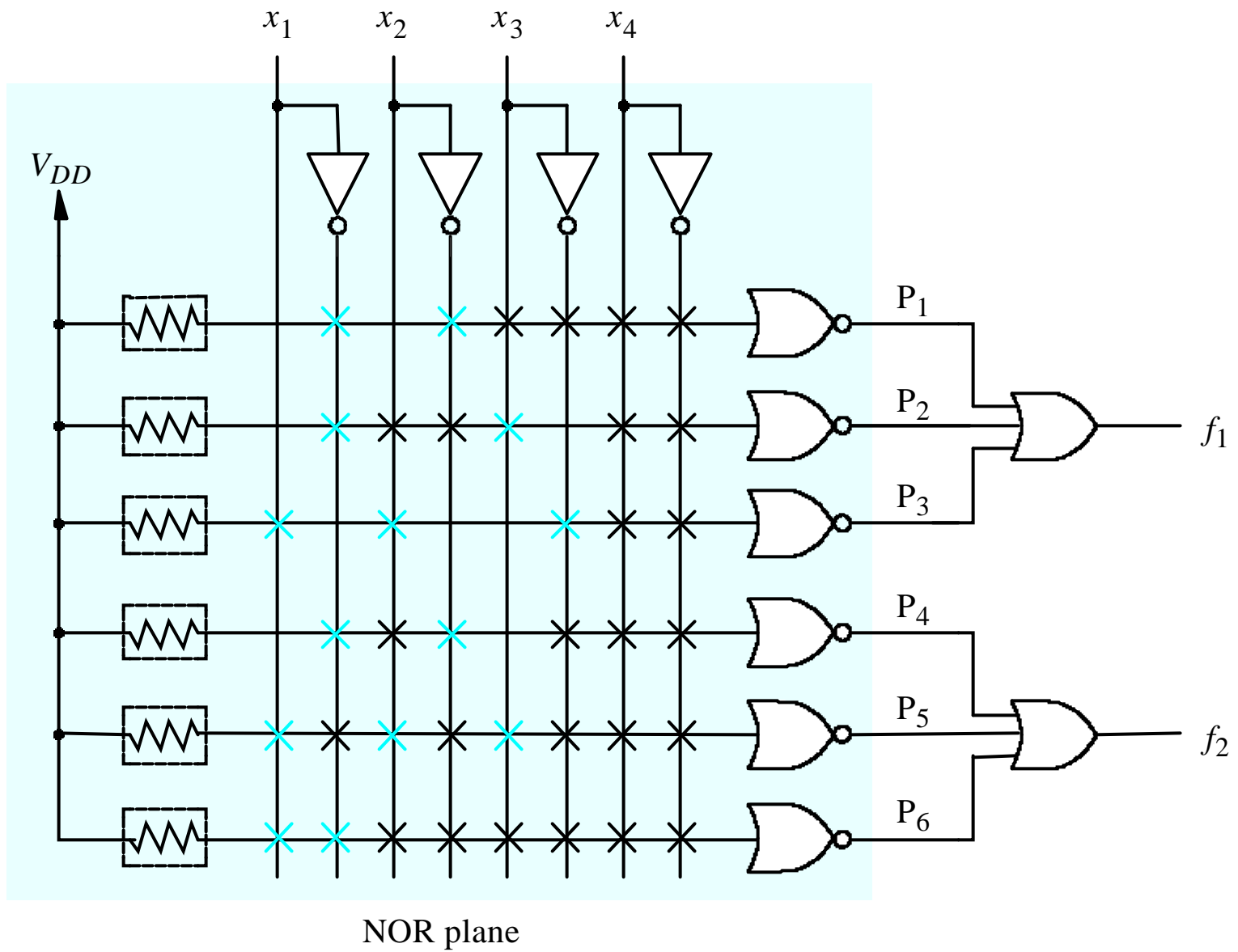
Figure 3.66 A NOR-NOR PLA used for sum-of-products

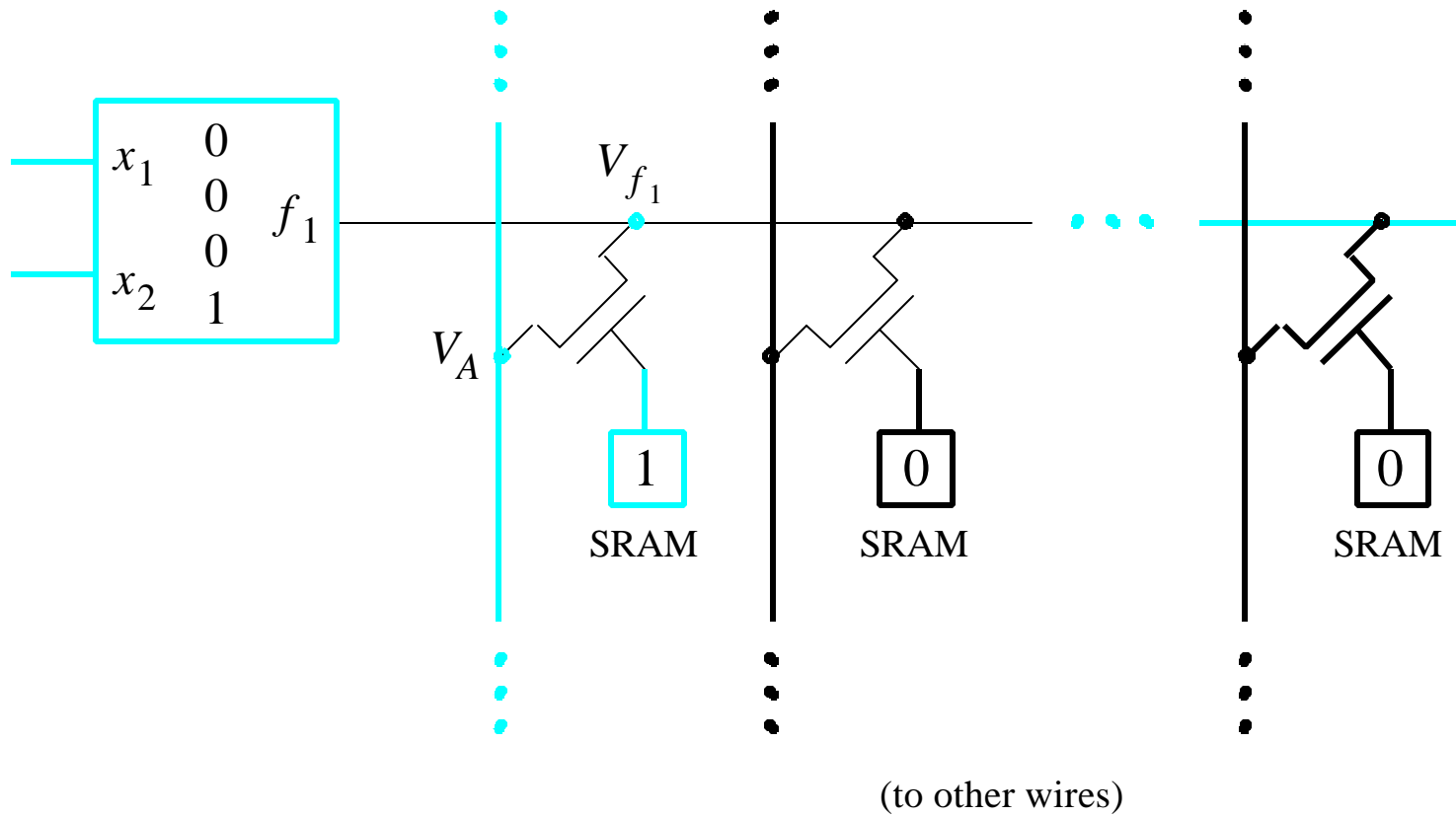Figure 3.67   PAL programmed to implement two functions
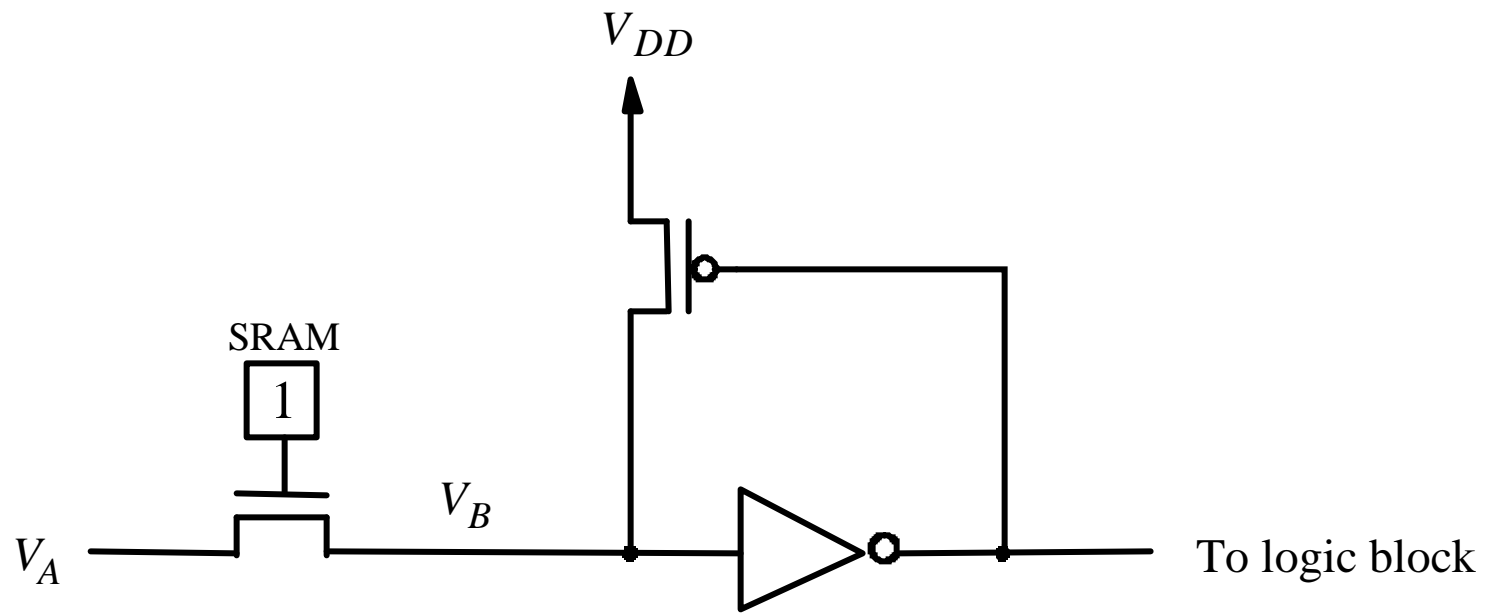
Figure 3.68   Pass-transistor switches in FPGAs
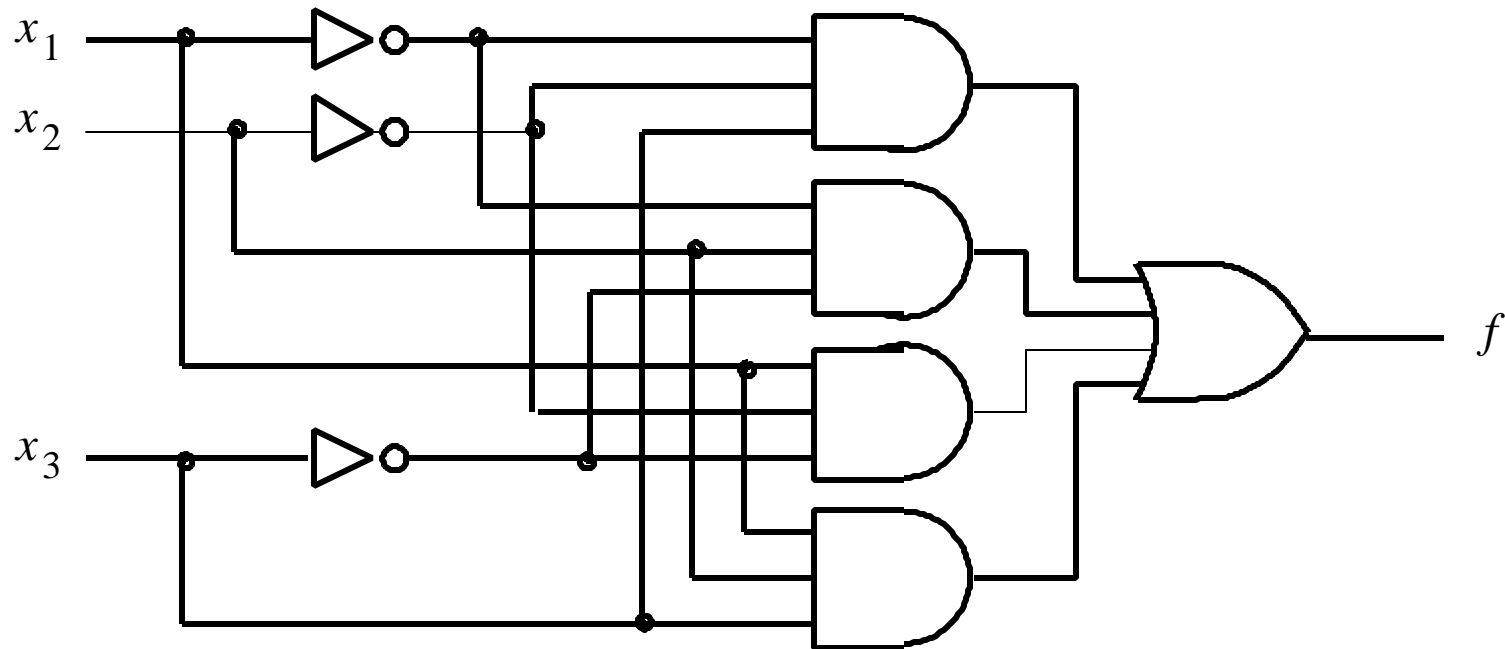
Figure 3.69   Restoring a high voltage level
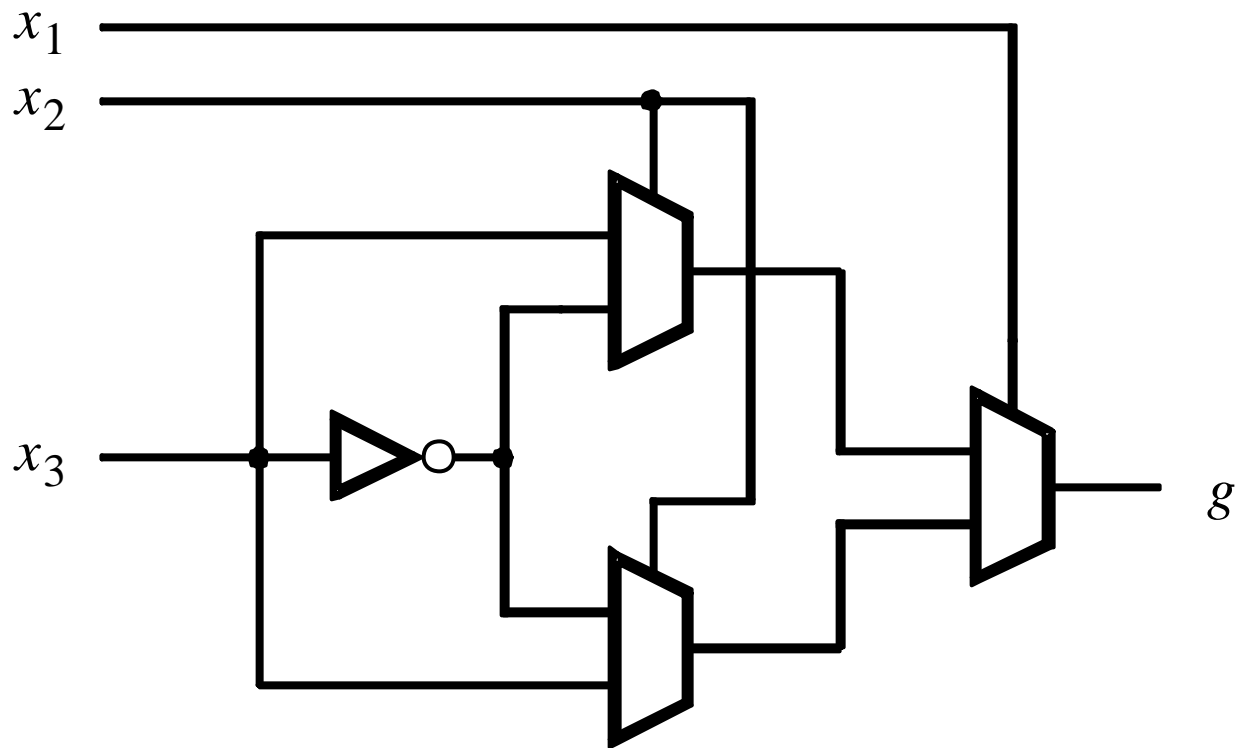
Figure P3.1   A sum-of-products CMOS circuit

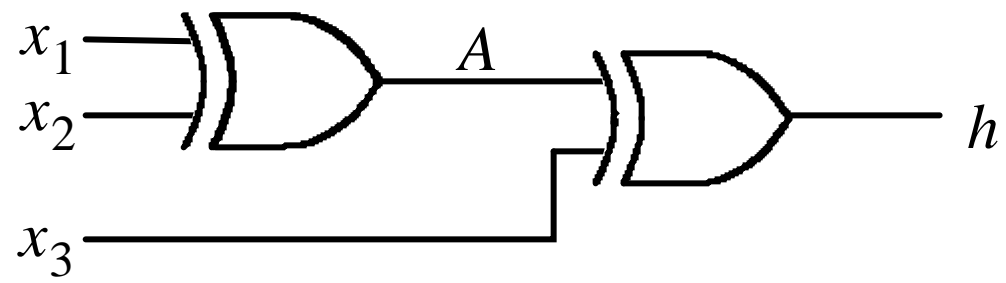Figure P3.2   A CMOS circuit built with multiplexers

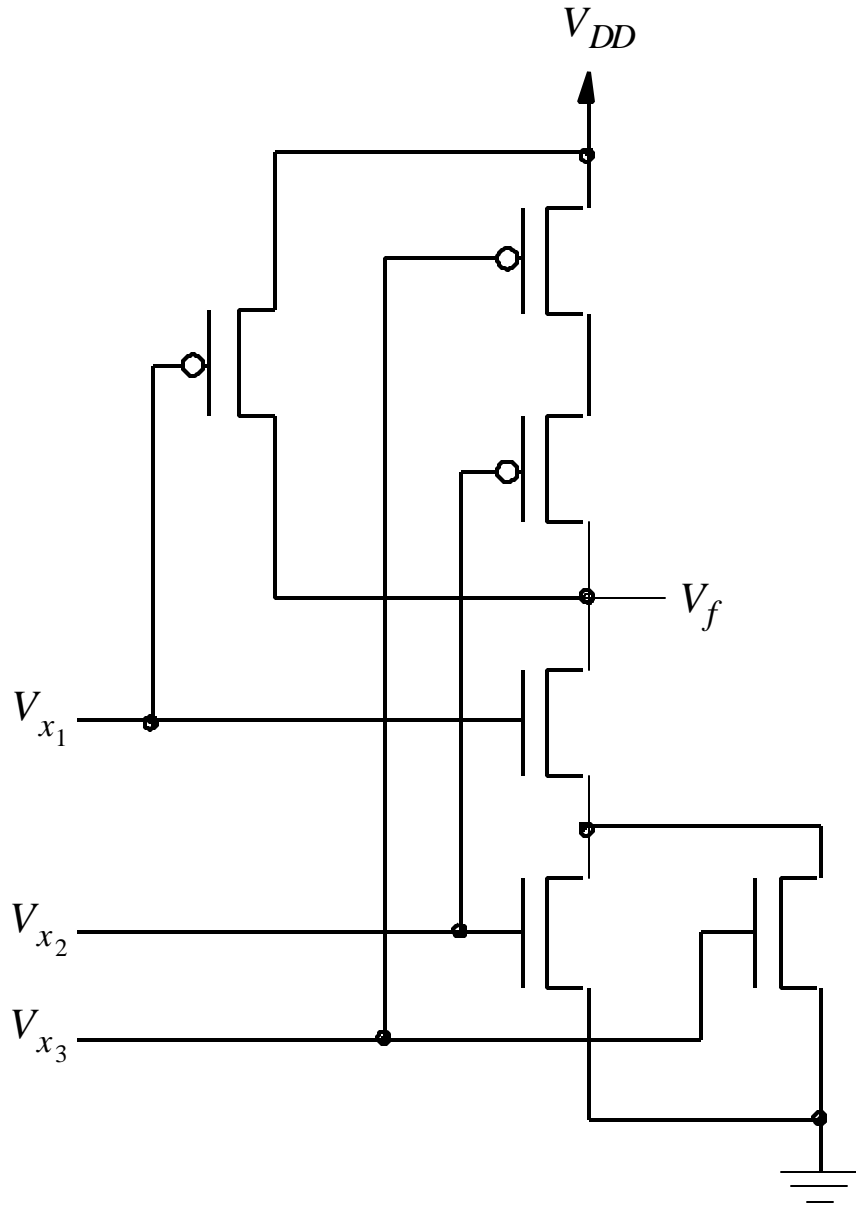Figure P3.3   Circuit for problem 3.3
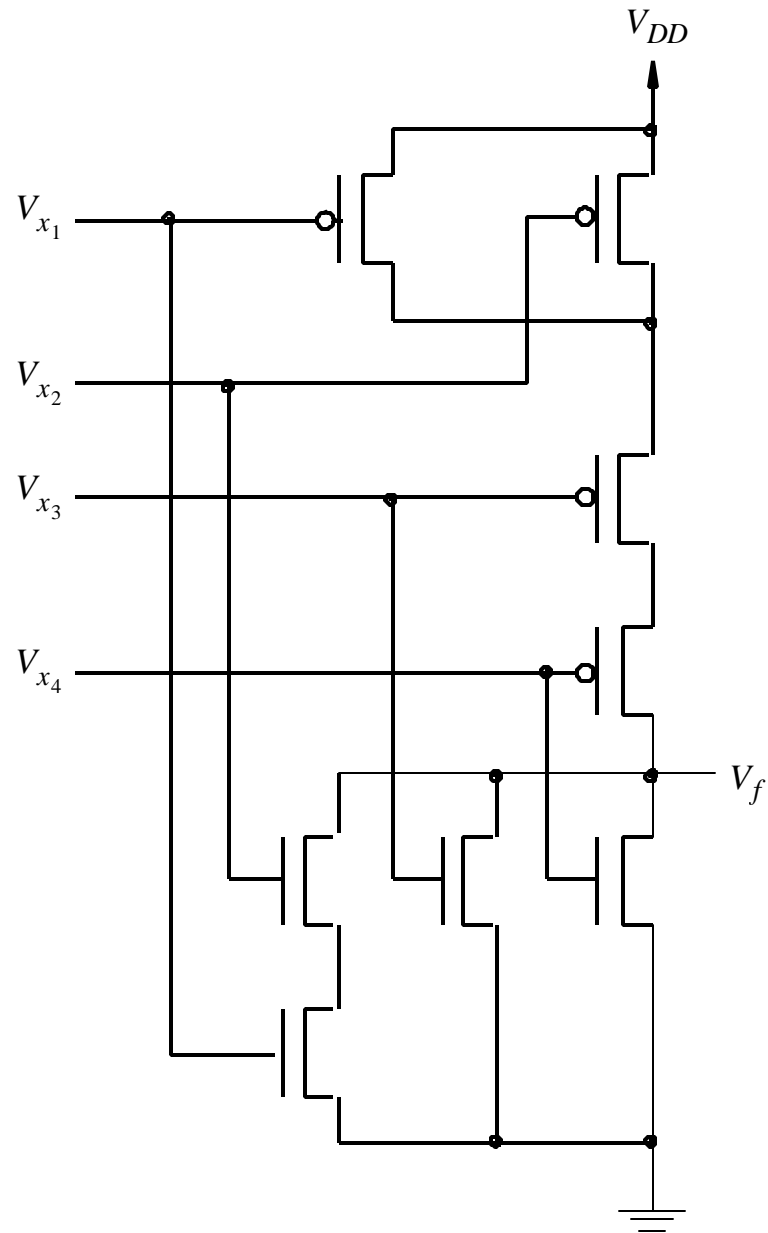
Figure P3.4   A three-input CMOS circuit

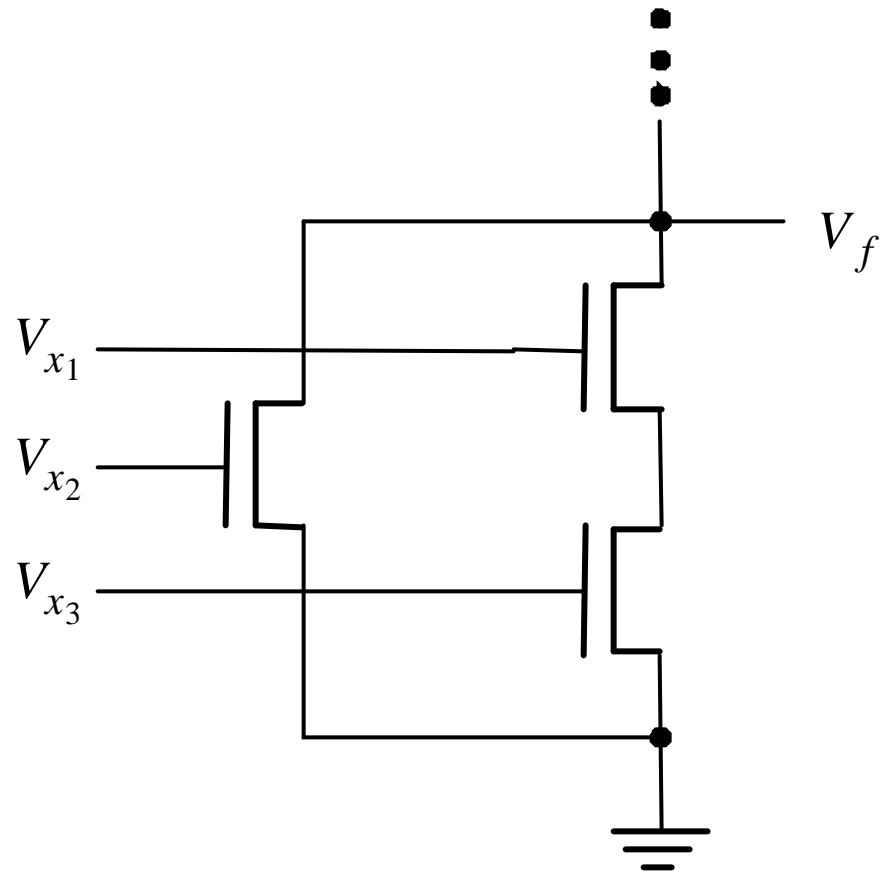Figure P3.5   A four-input CMOS circuit

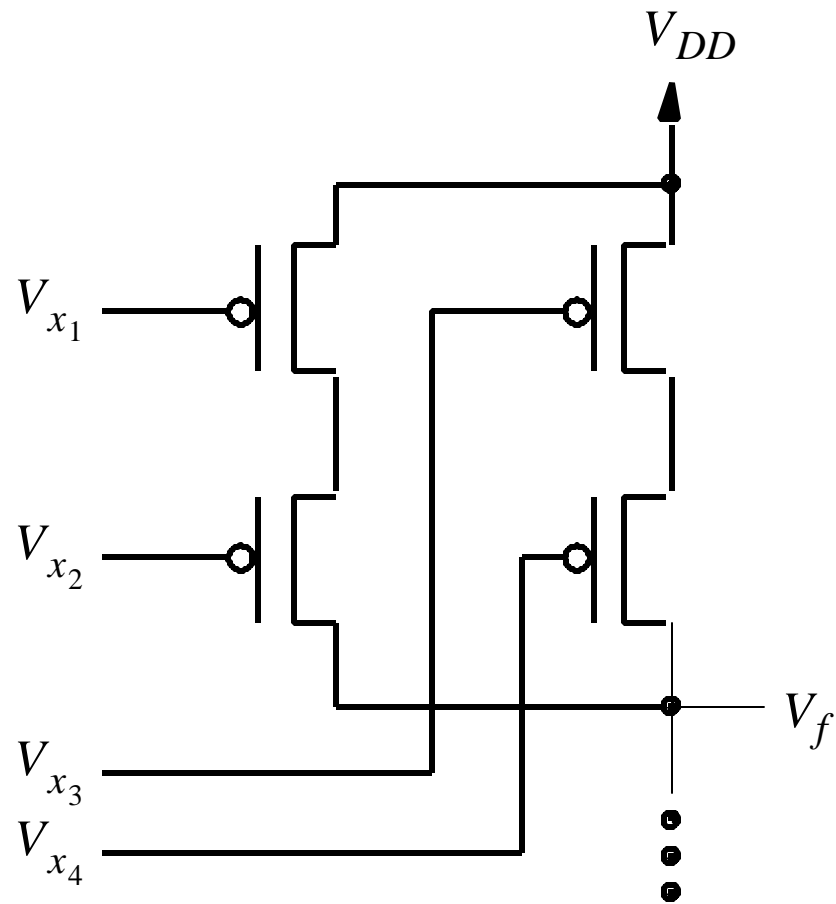Figure P3.6   The pull-down network in a CMOS circuit

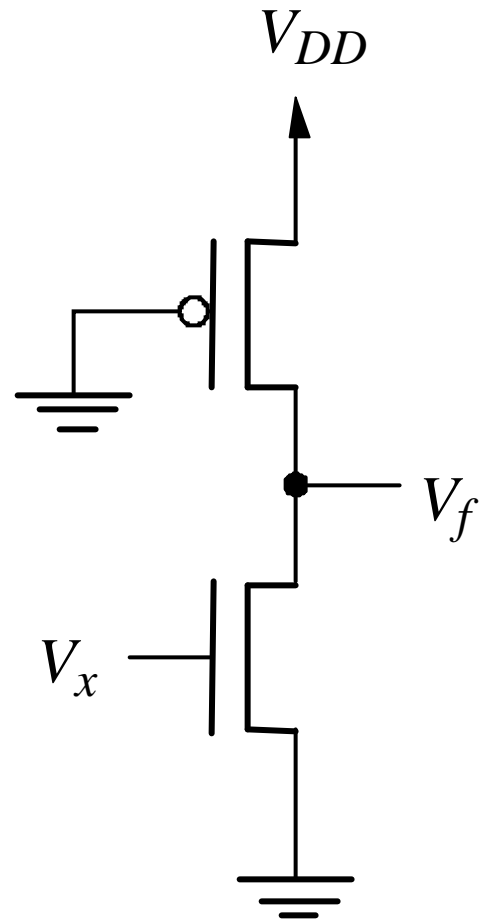Figure P3.7   The pull-up network in a CMOS circuit

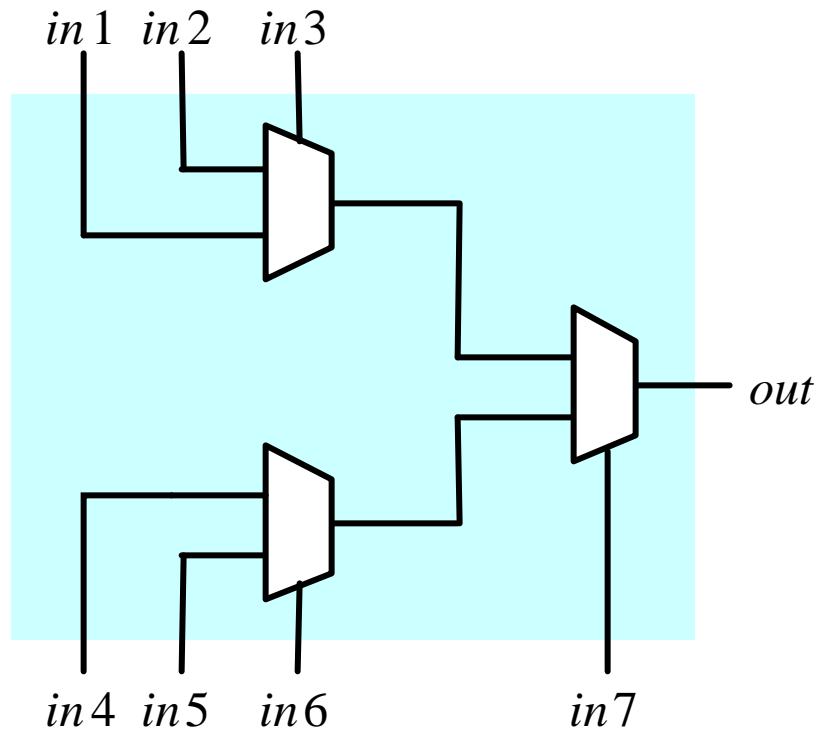Figure P3.8   The pseudo-NMOS inverter
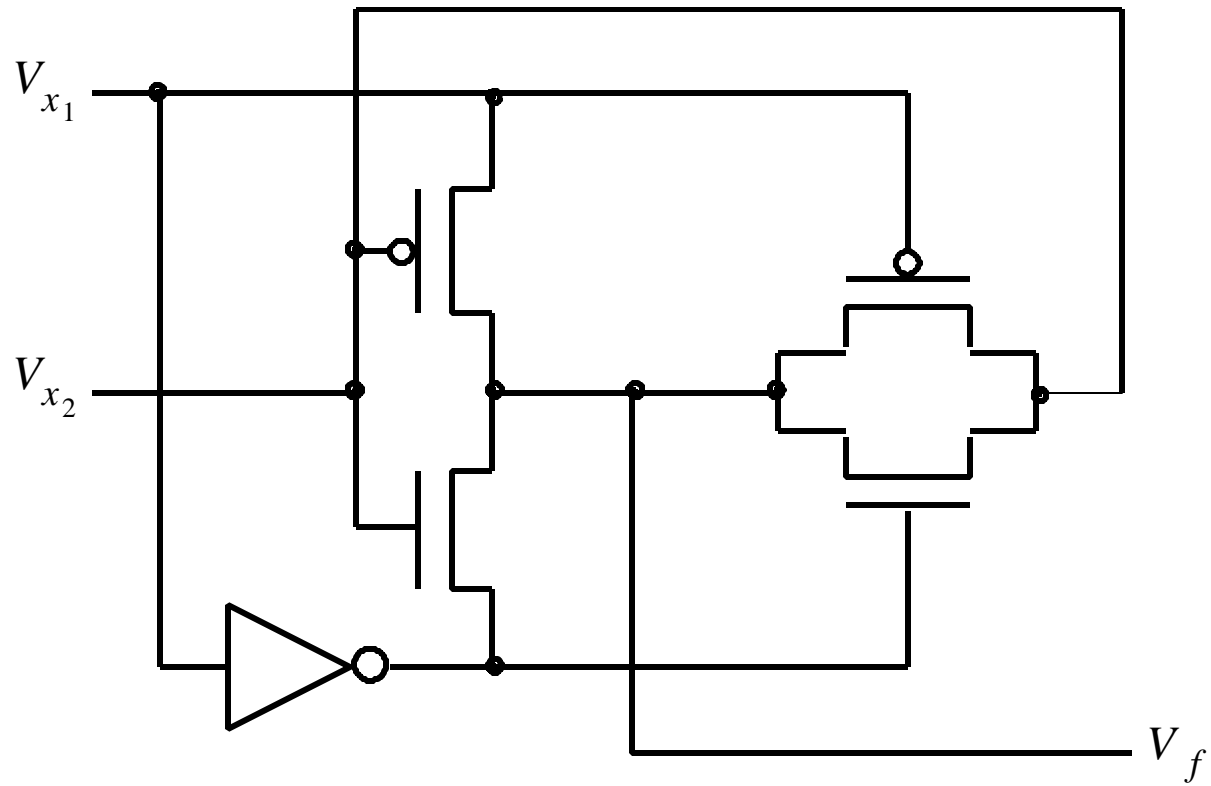
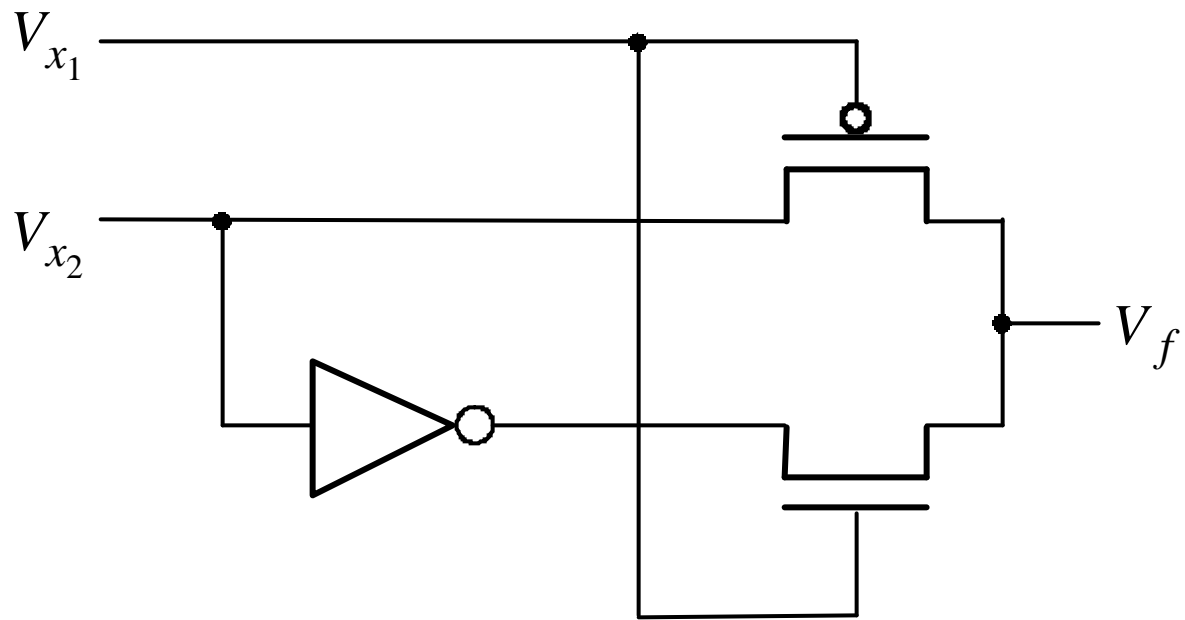Figure P3.9   A gate-array logic cell

Figure P3.10   Circuit for problem 3.54

Figure P3.11   Circuit for problem 3.55